

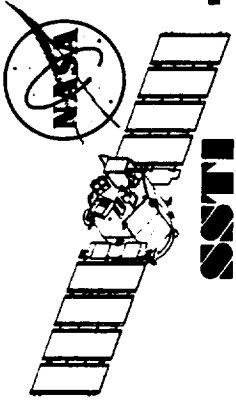
Integration and Test



Spacecraft System Integration and Test

Spacecraft System Integration and Test SSTI Lewis Critical Design Audit

R.P. Brooks
K.K. Cha
1-18-95



Integration and Test Purpose and Objectives



Assemble, integrate, and test the SSTI spacecraft in a manner which provides the most efficient and effective means for achieving program objectives

I&T test objectives

- Execute a test program which demonstrates high probability that the spacecraft will meet on orbit mission requirements
- Deliver to the launch site a fully integrated, tested, and operational spacecraft 24 months after ATP

Basic integration and test approach

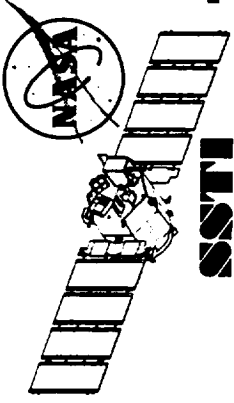
- Develop a system level test program based upon proven verification processes performed on all TRW programs

- Referenced to GEVS, Mil-Standards and commercial practices (TDRS 1-7 ----->TOMS --->STEP--->Odyssey)

* Thermal cycling, thermal vacuum, thermal balance tests

* EMC/EMI, 3 axis random vibration, solar array 1st motion release

(Note: structure development tests and solar array full deployments tests covered in Structures and Mechanisms section)



Integration and Test Purpose and Objectives

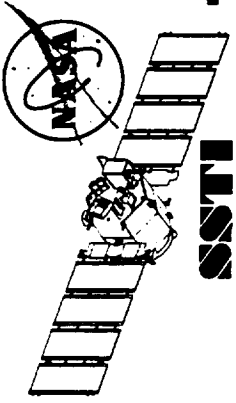


Basic integration and test approach (cont'd)

- Effectively utilize all available program design and test organizations
 - Co-locate major integration and test activities with those resources
- Implement within program constraints lessons learned from existing NASA, TRW, and DoD programs
- Assess viability of process improvement studies on new and existing TRW programs
 - AXAF, TDRS 1-7, DSP, BE, TOMS, STEP, Rocsat, Komsat, Odyssey, TDRS H, I, J, EOS, and Advanced Bus
 - Integrated Product Teams

Colocate major integration and test activities with program proper resources

- SSTI modular design enables parallel integration and test
 - Payload Module (Tech Demo's) at TRW Chantilly, Va.
 - Avionics Module at TRW Space Park, Ca.
 - Battery/Propulsion Module at TRW Space Park, Ca.



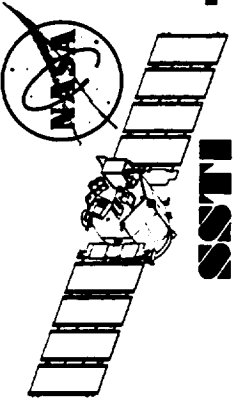
Integration and Test Module Integration Approach



Co-locate major integration and test activities with proper program resources

Payload Module integration and test

- Assemble, integrate, and test Payload Module at TRW Chantilly facility
 - Convenient access for most Tech Demo instrument design and development organizations
 - * GEM (SLAM, MMHS, MM Accels, Solar Cell), GPS Attitude, WFOV STA, Rad. Monitor, and PEA
 - * LEISA and OPA (if schedule permits)
 - ** SSR-BB
 - Utilize integration and test capability at TRW Chantilly facility
 - System Test Engineering and Test Operations
 - ** TRW and J&T
 - * EGSE and MGSE Engineering design and fabrication
 - Certified test facilities (STEP, AB600)



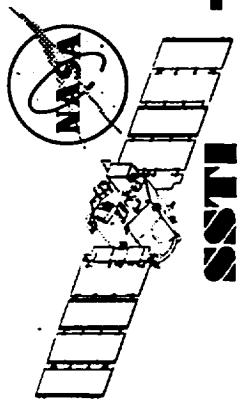
Integration and Test Module Integration Approach



Co-locate major integration and test activities with proper program resources

Payload Module integration and test (cont'd)

- Develop test requirements, test procedures, EGSE, simulators, test software, and MGSE
- Install electrical harness, 1553B, thermistors, test instrumentation, and structural components
 - Integrate and functionally test Tech Demo instruments and LEISA (schedule permitting)
 - Thermal cycle test (if schedule permits)
 - Ship to Space Park as an assembled and tested module
- Evaluate data remotely via T1 line during spacecraft system level tests conducted at TRW Space Park

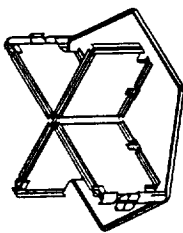
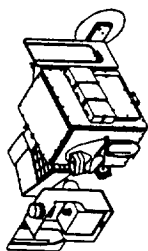


Spacecraft Modularity

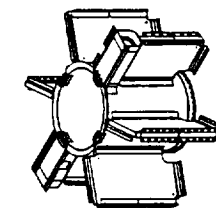
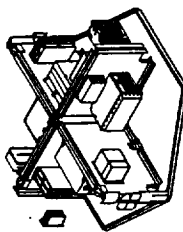


MODULE ASSEMBLY

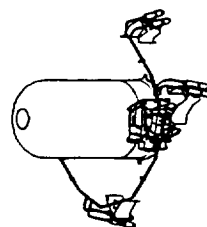
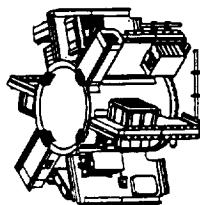
INSTRUMENTS



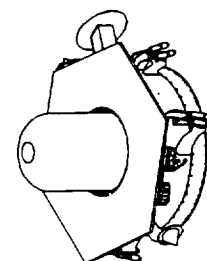
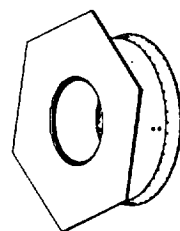
PAYLOAD
MODULE



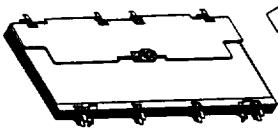
AVIONICS
MODULE



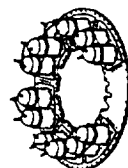
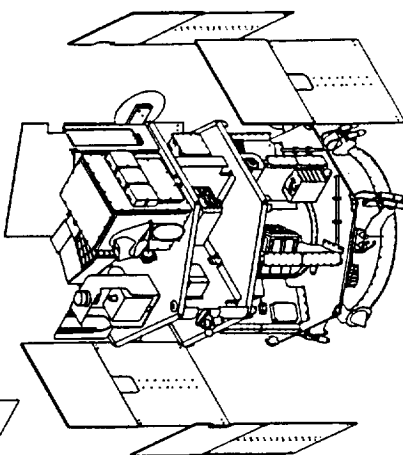
BATTERY PROPULSION MODULE



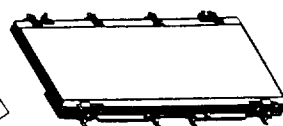
I&T-6

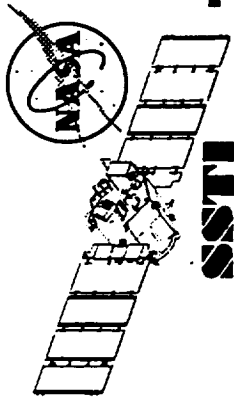


FINAL
ASSEMBLY



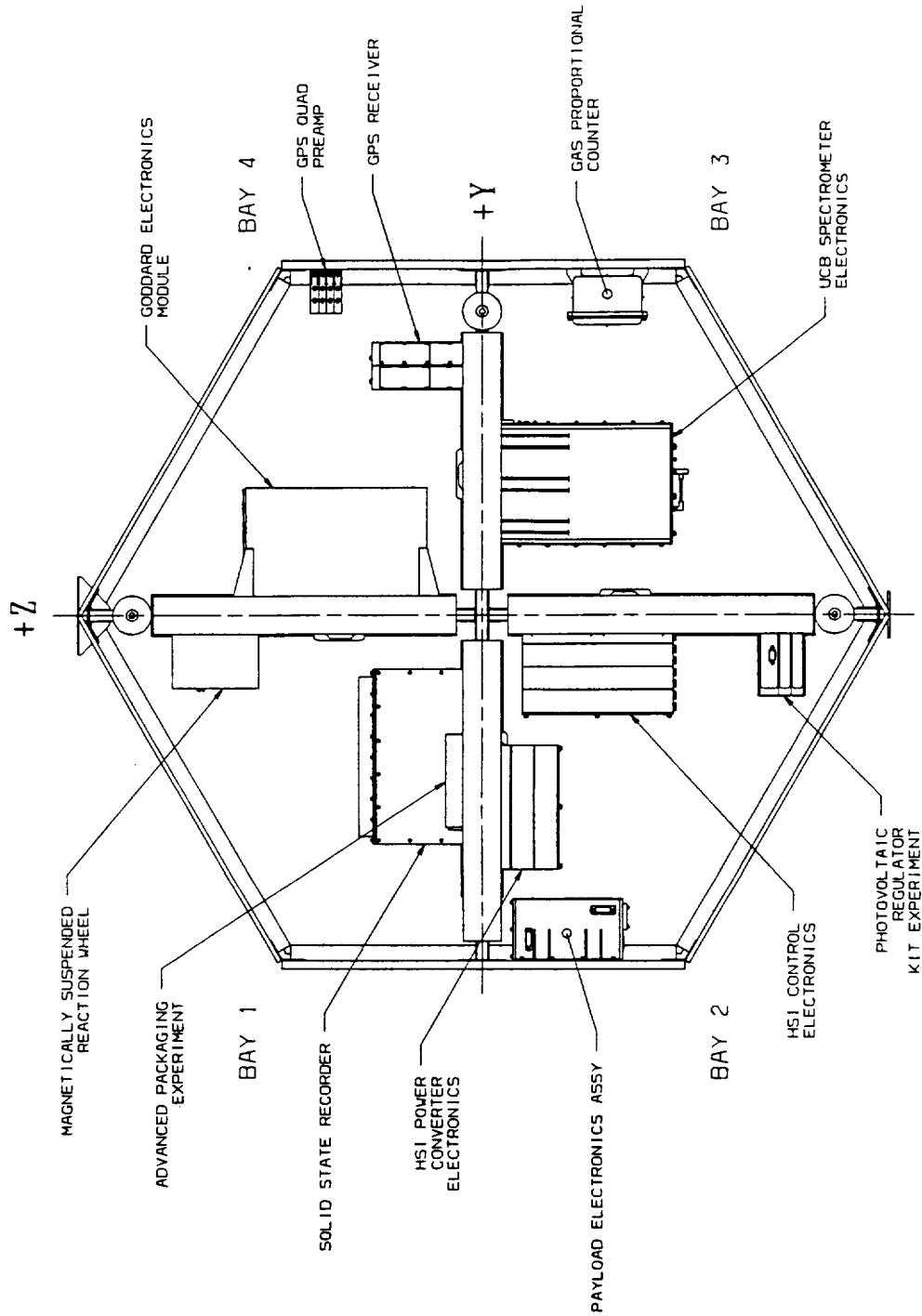
BATTERY
MODULE



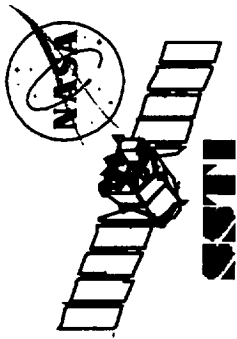


Payload Module Layout

Plan View



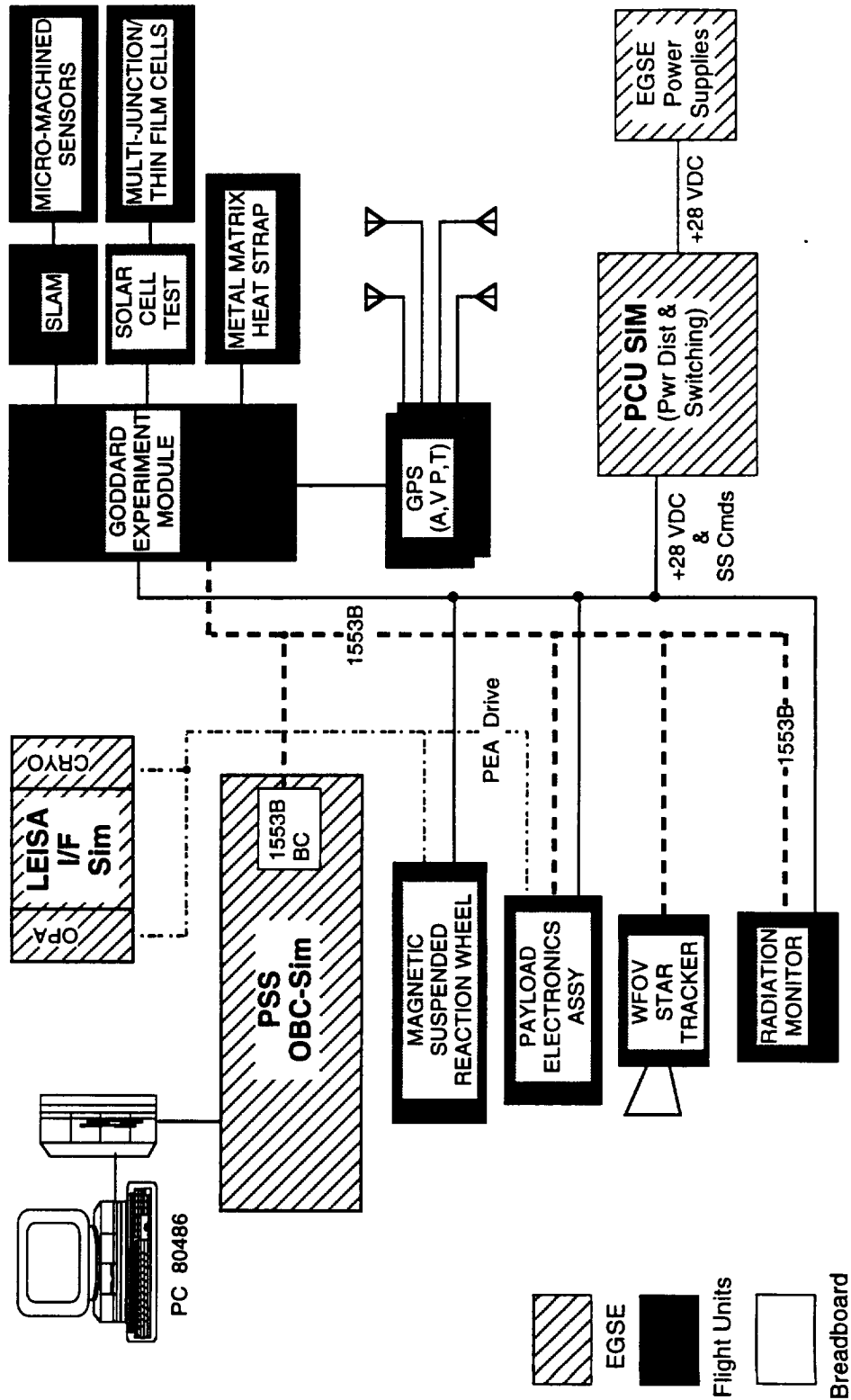
VIEW LOOKING -X
(INSTRUMENT PANEL REMOVED FOR CLARITY)

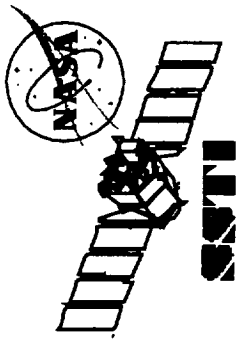


Integration and Test



Payload Module Test Configuration-1 (instrument integration)

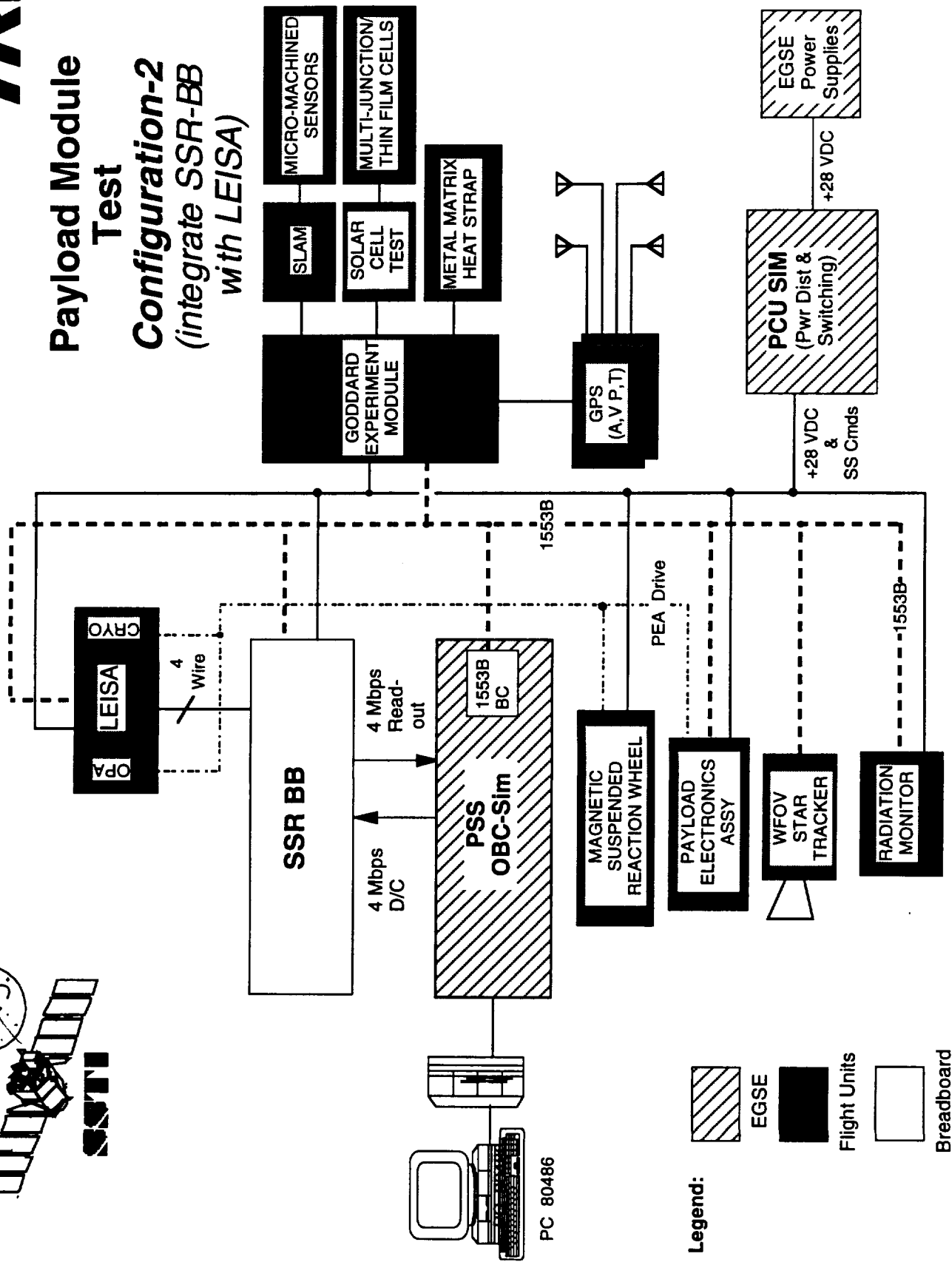


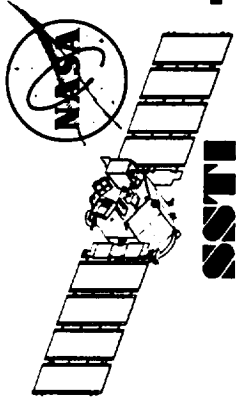


Integration and Test



Payload Module Test Configuration-2 (integrate SSR-BB with LEISA)





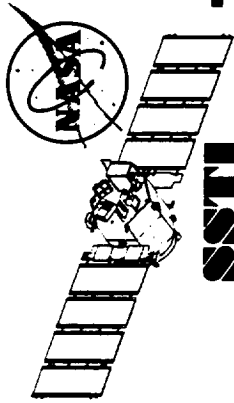
Integration and Test Module Integration Approach



Co-locate major integration and test activities with proper program resources

Avionics and Battery/Propulsion Modules integration and test

- Assemble, integrate, and test AM and BPM at TRW Space Park facility
- Convenient access for subsystem design and development organizations
 - * DMS, EPDS, ACS, and OAS subsystems
- Utilize integration and test capability at TRW Space Park facility
 - Spacecraft System Design and Integration

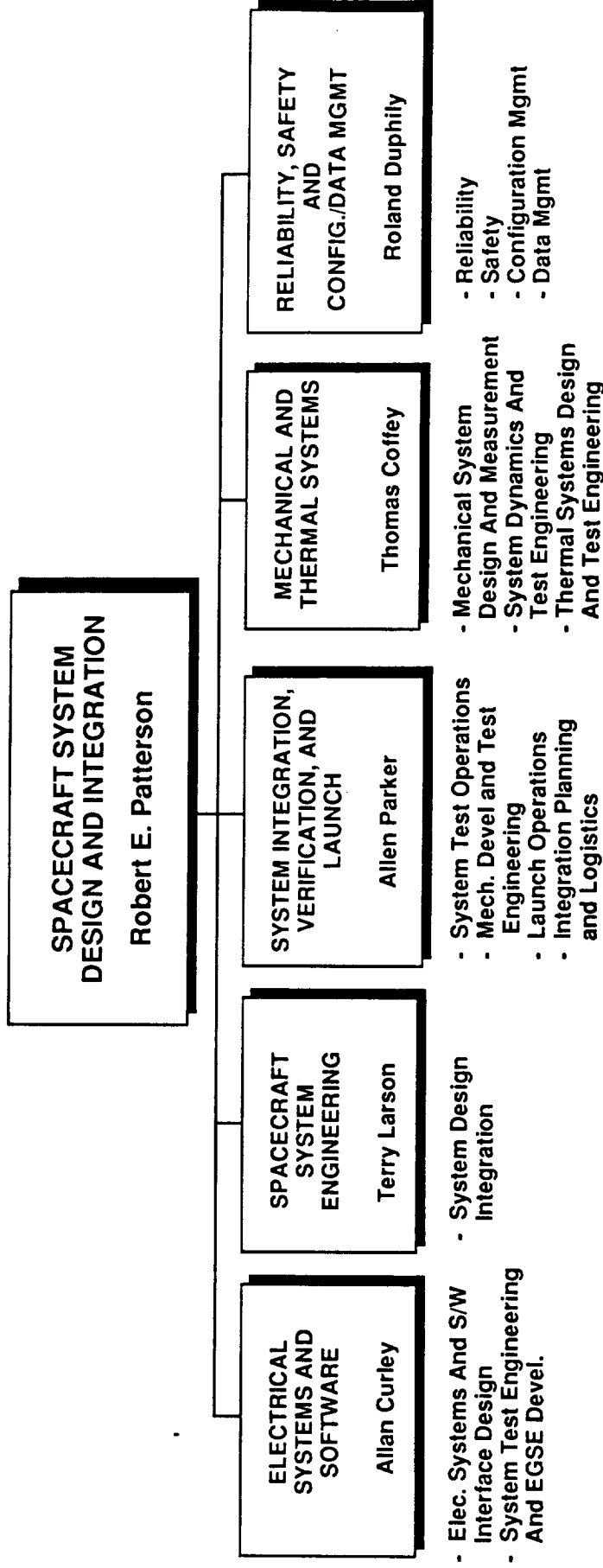


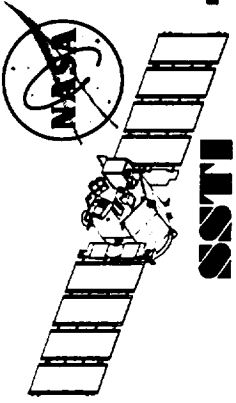
Integration and Test

Spacecraft System Design and Integration

*SSTI Spacecraft Integration and Test will be performed at Space Park,
Redondo Beach, Ca.*

Space Park integration and test resources





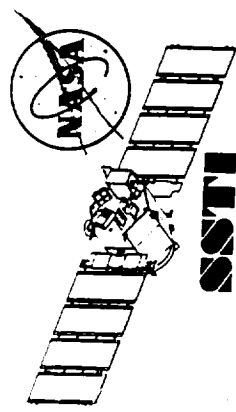
Integration and Test Spacecraft Integration and Test



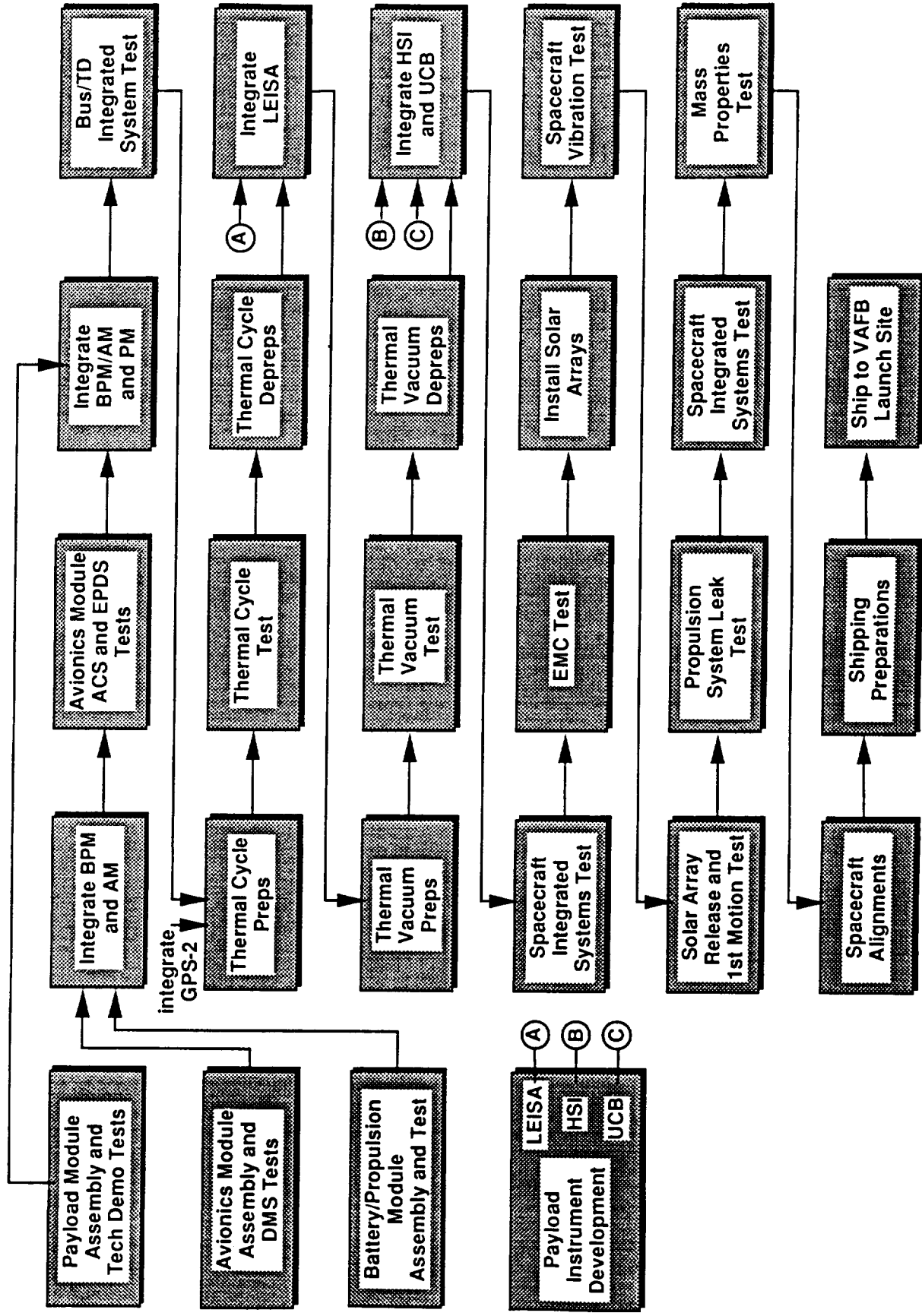
Co-locate major integration and test activities with proper program resources

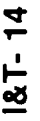
Spacecraft System Design and Engineering Center supported with sustaining design engineering at Space Park throughout test program

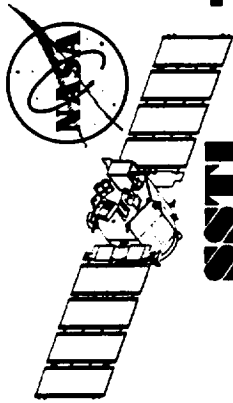
- DMS engineering support (component design, development, and test)
 - OBC (R3000), SSR, and DIU
- EPDS engineering support (component design, development, and test)
 - SARE, PCU, and DDC
- ACS engineering support (component design, development, and test)
 - TAM, ESA, CSSA, GRA, CEA, RWA, NFOV STA, VDE, and T-Rods
(Design responsibility is at Chantilly. Space Park Control Lab provides support during I&T)
- HSI engineering support (design, development, and test)
 - Focal planes and mechanical systems, HPE, HCE, and Cryocooler
 - PEA, OPA (LEISEA) and Cryocooler
- UCB, LEISA, and Tech Demo support as required (design, development, and test)



Integration and Test Flow



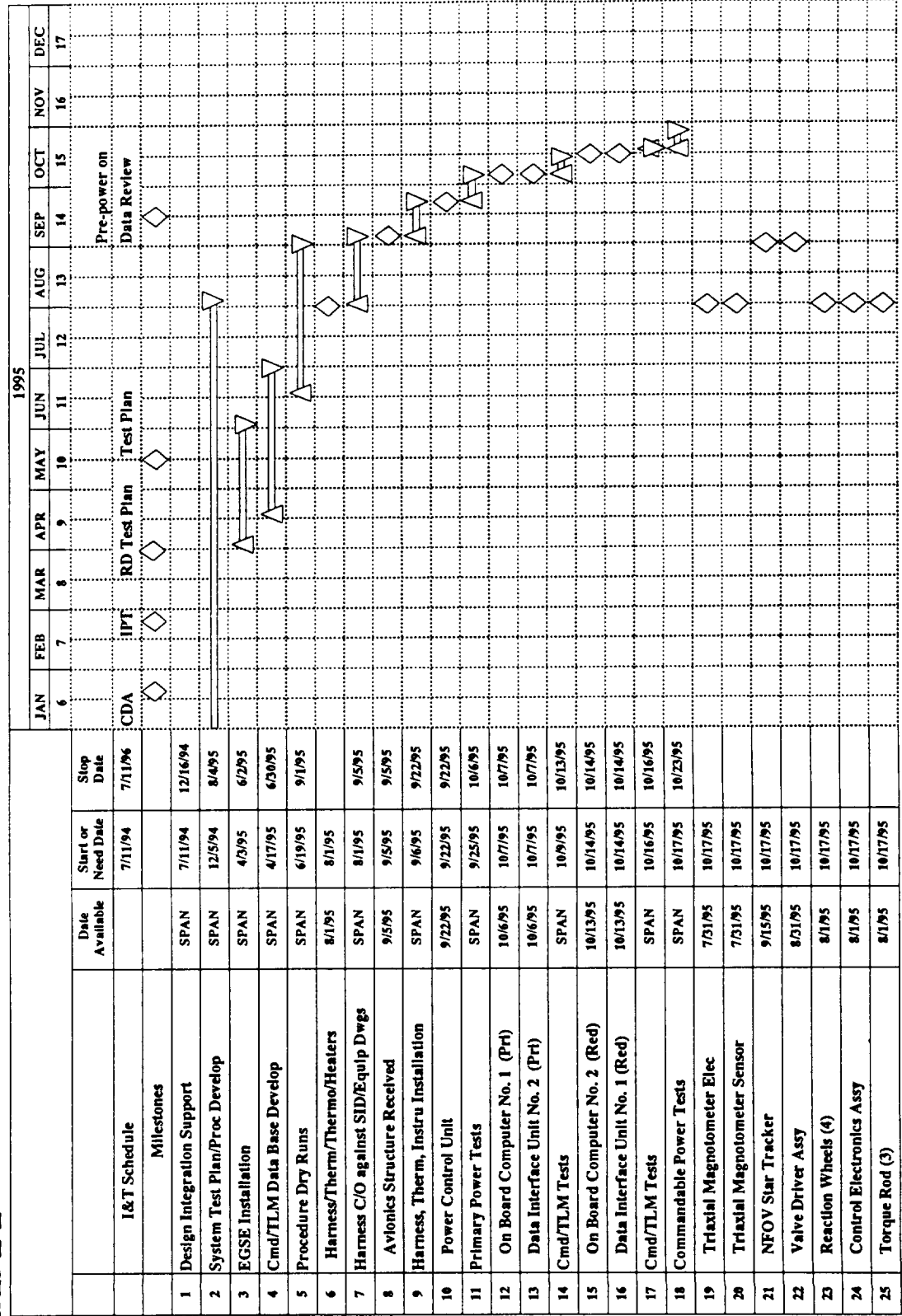
**IN 20**

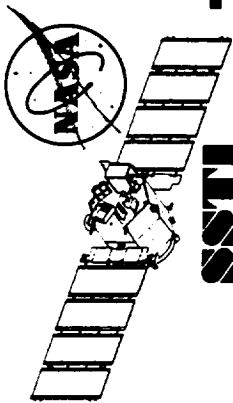


Integration and Test Schedule

TRW

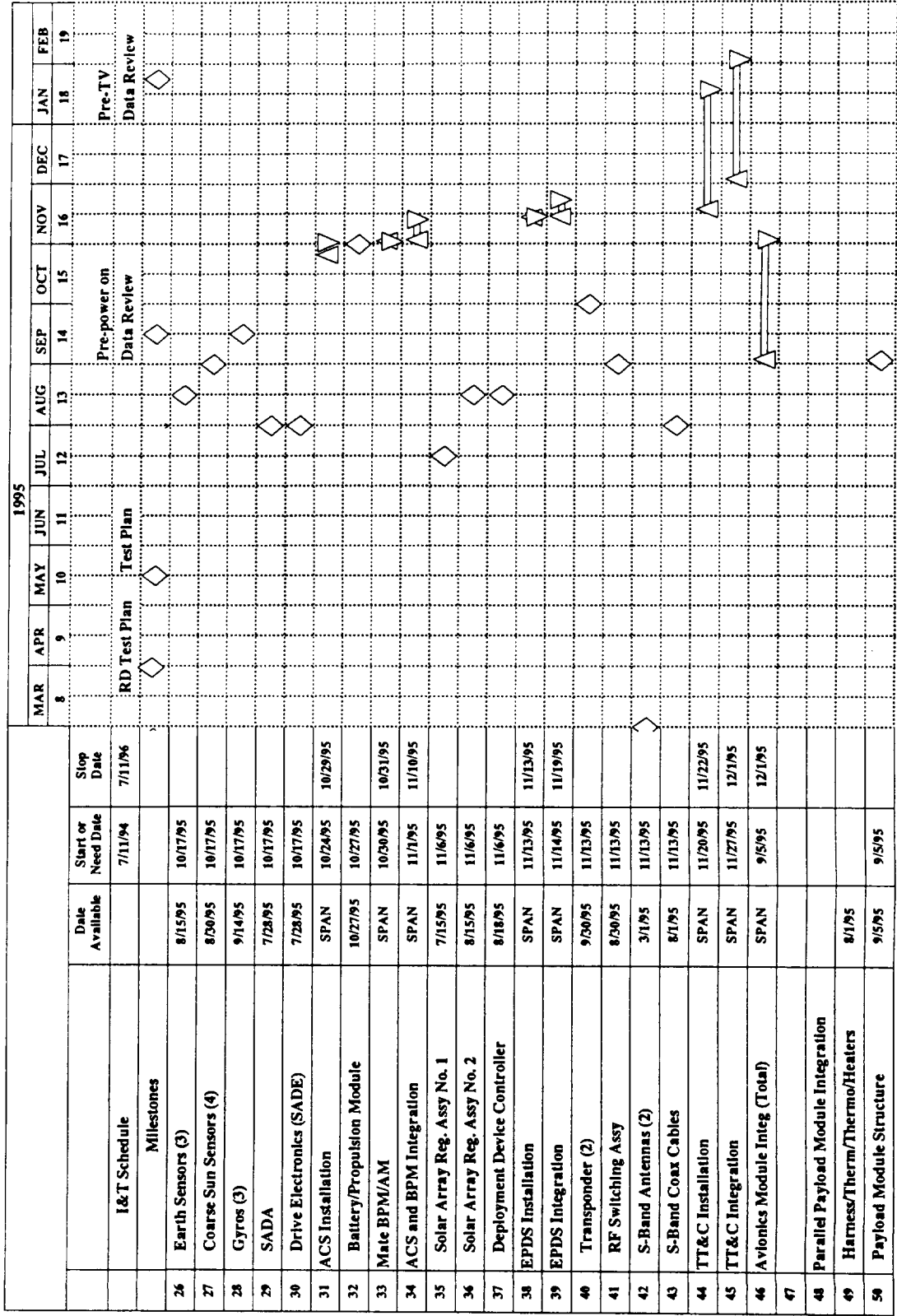
SSTI

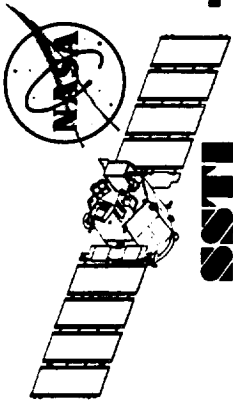




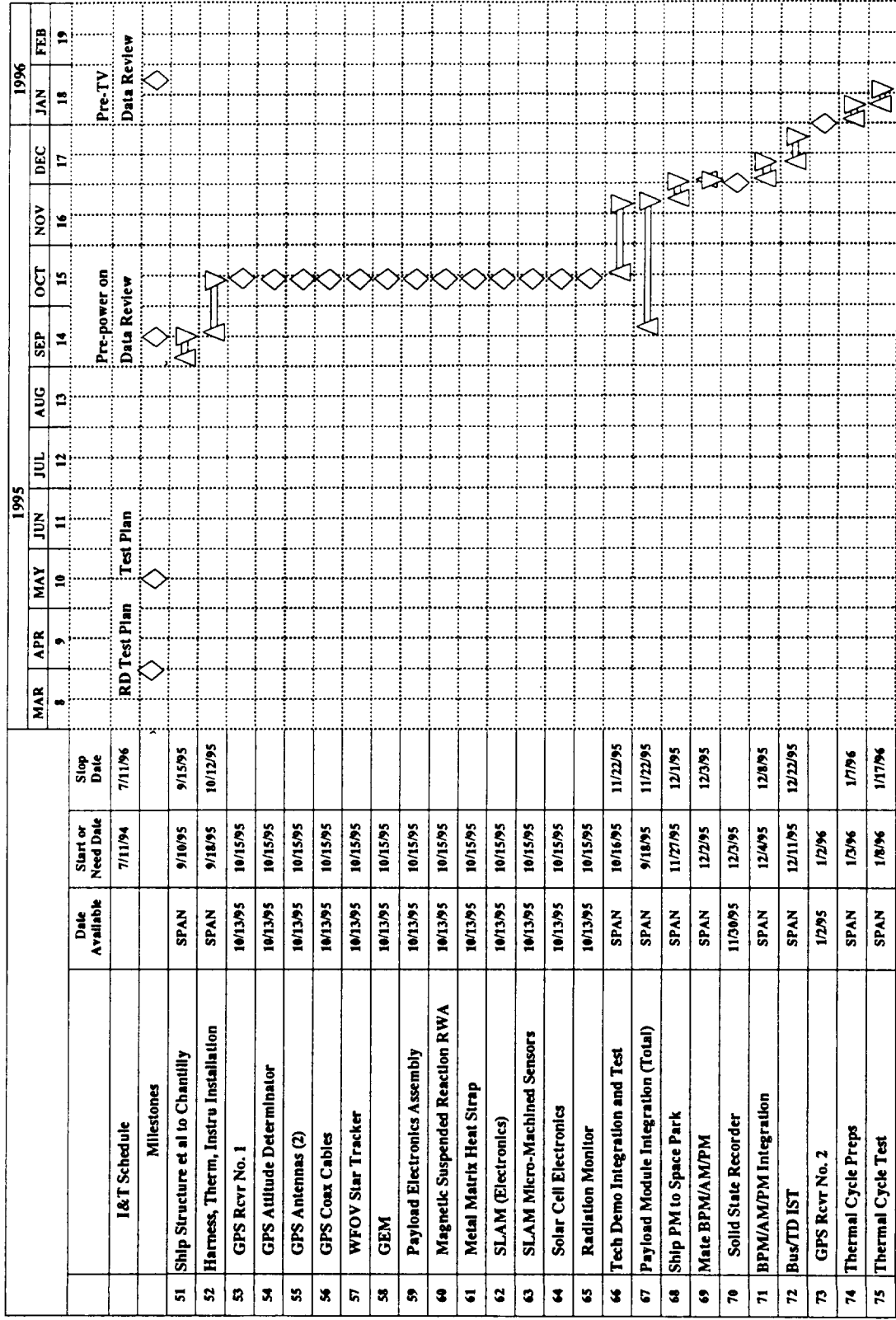
Integration and Test Schedule

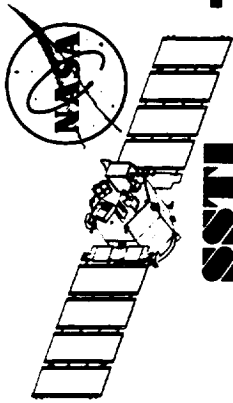
TRW



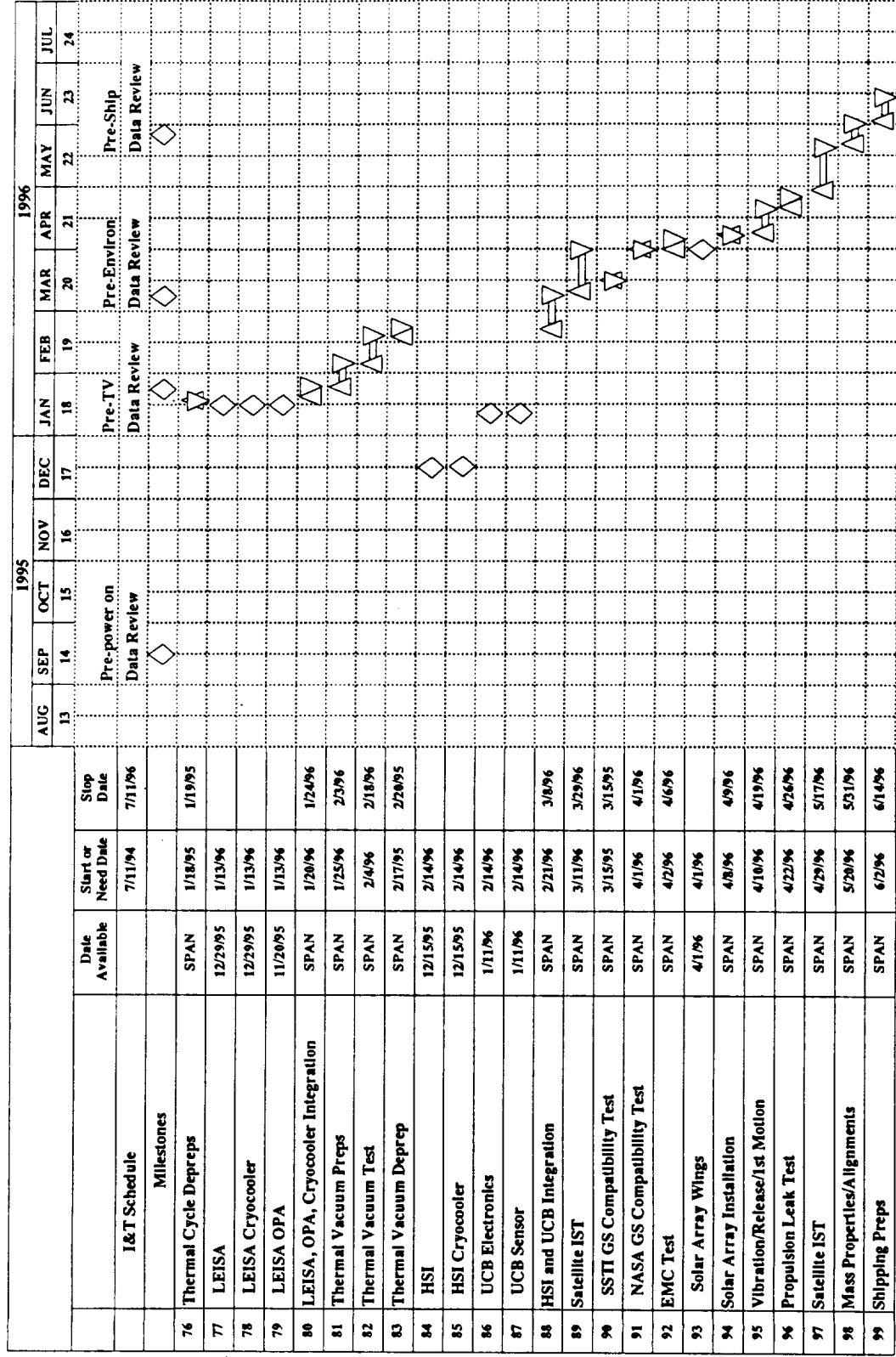


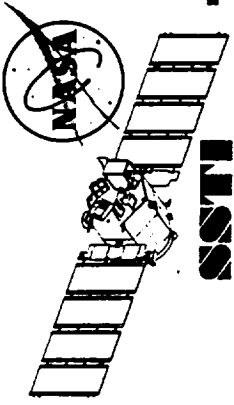
Integration and Test Schedule





Integration and Test Schedule



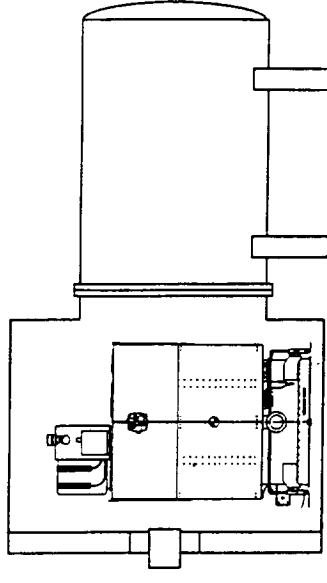


Integration and Test Thermal Vacuum Test



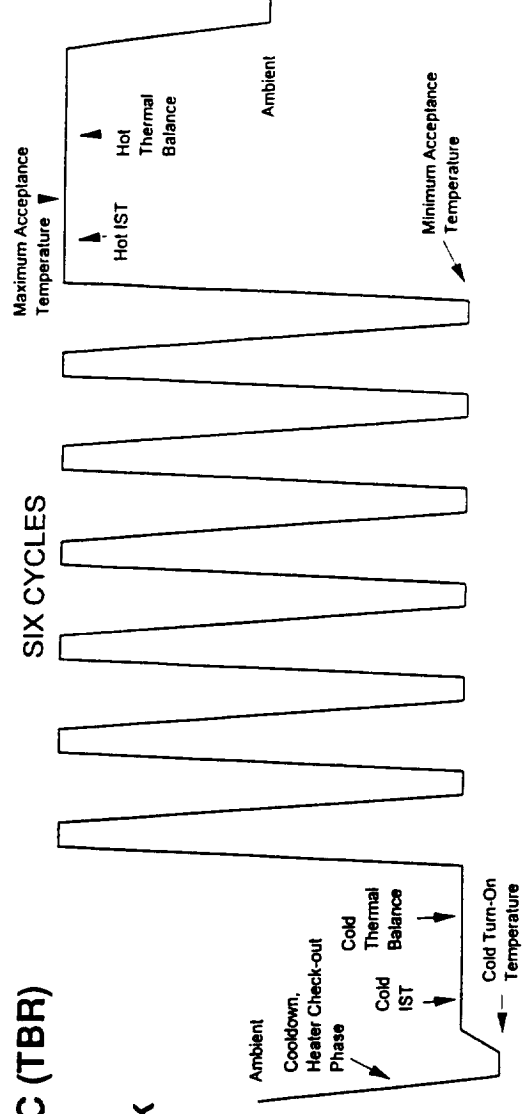
Test requirements

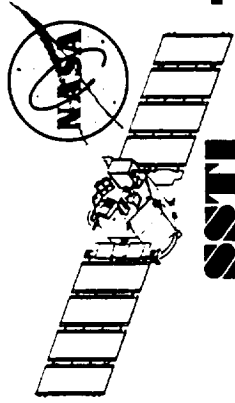
- Flight configuration with the following exceptions
 - Solar arrays not installed
 - UCB and HSI not installed
 - LEISA installed and integrated (not presented to CCB)
- Spacecraft powered on in ascent configuration during pumpdown (TBR)
- Cold and hot balance with six cycles
- Spacecraft temperatures limits
 - Min/max predicted for flight plus 5° C (TBR)
- Spacecraft Integrated System Tests
 - IST's performed at cold and hot soak



Thermal Chamber (M4 facility)

- Horizontal cylinder with hammerhead extension
 - LN² shroud with cryo pump





Integration and Test Spacecraft Vibration Test

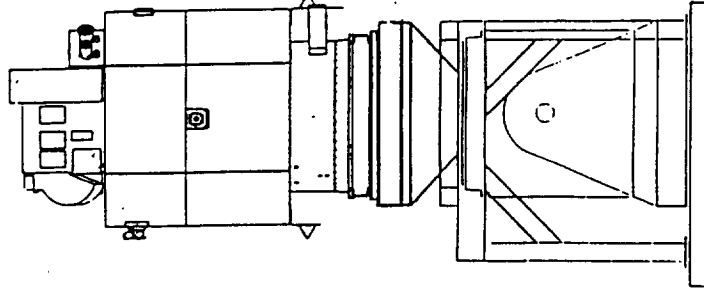


Test requirements:

- Full flight configuration less thermal blankets
 - Solar arrays installed
- Spacecraft powered on in launch and ascent configuration
 - SLAM data taking during one single axis test
- Three axis random vibration, one axis at a time
 - Test duration one minute per axis
- Spacecraft integrated system tests performed
 - Pre and post vibration

Vibration system:

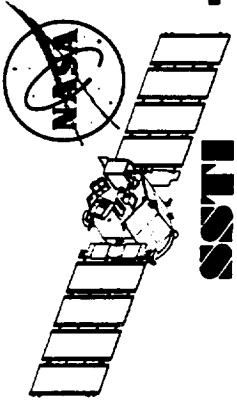
- Unholz-Dickie T-4000 electrodynamic exciter, 40k force lbs-100g, 1.75" stroke
- Oil film and hydrostatic bearing systems for lateral axis tests
- LMTS advanced digital vibration control system with 16 channel data acquisition system



Spacecraft Acceptance Test Induced Random Vibration Levels

Spacecraft Acceptance Test Levels		
Frequency (Hz)	Acceleration Spectral Density (G^2/Hz)	
20.0	0.002	
100.0	0.040	
800.0	0.040	
1475.0	0.016	
2000.0	0.016	

Overall Levels	
Acceptance	7.56 Gms



Integration and Test

EMI/EMC System Verification Test



SYSTEM TEST OBJECTIVE

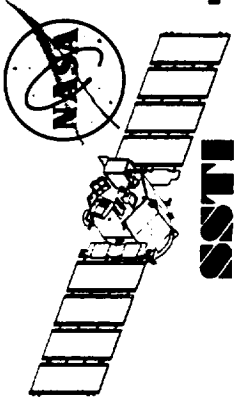
- Demonstrate spacecraft self-compatibility (including instruments) and compatibility with the launch site and launch vehicle environments

TEST LOCATION

- TRW, Redondo Beach, Building - 108C (Certified EMC Test Facility)

PLANNED TESTS

- Measure satellite self-generated radiated interference between 1-3 GHz (around S-Band Receiver frequencies).
- Ensure levels meet the "Notch" defined in figure A-5 and A-6 of the SR1-0125 Document (EMC Specification).
- Subject satellite to the radiated susceptibility signals
 - The SSTI S-Band Xmitter (Figure A-7 in SR1-0125
 - Other transmitters levels associated with launch vehicle (LLV1) or launch site (VAFB).
 - Verify nominal satellite operation during exposures.



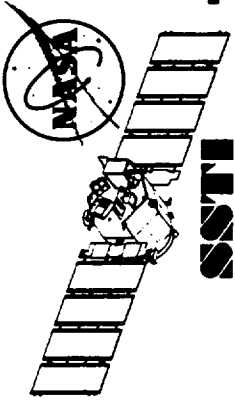
Integration and Test Spacecraft Integration and Test



All test facilities and major test equipment have been identified

TDRS 1-7 high bay is available March 1995

- M2/1568 Integration and test area
 - Class 100k (filtered air) - utilize TOMS tent for payload integration
 - Portable thermal cycling chamber in high bay
 - Module/subsystems initially integrated on chamber platform
 - 6400 square feet integration area
 - 2 ton crane (26' hook height)
 - Co-located office space
- M1/1581 Dynamics area
 - 3 axis random vibration test performed
 - Propulsion/leak test in acoustic chamber
- M4 Thermal Vacuum Area
 - Thermal vacuum/balance test performed
- Bldg 108C EMC/EMI Test Area
 - System level EMC test performed



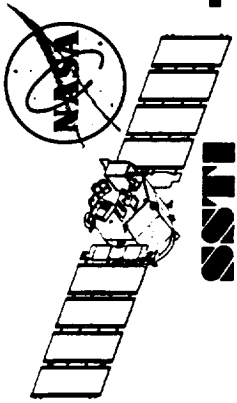
Integration and Test Spacecraft Integration and Test



Integration and Test status

Near term tasks

- Review I&T schedule with functional organizations
- Develop SSTI manpower loading plan
 - EGSE and MGSE design and development
 - * ISATS, simulators, and test beds
 - * ISATS data base development
 - * Test software development
 - Develop System Test Plan Document D22877
 - * Rough draft release March 31, 1995
 - * CADM release May 12, 1995
 - Test procedure development
 - Test operations support and training
- Determine costs for environmental test support
- Schedule IPT meeting to baseline I&T program
 - Delta CDA February 21, 1995
- Coordinate Payload Module integration tasks with Chantilly I&T



Integration and Test Spacecraft Integration and Test



ICDA-2 Action Item Status

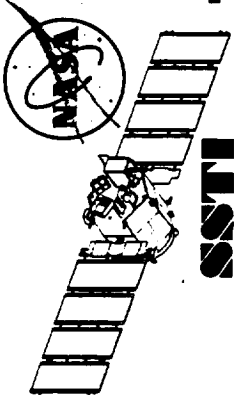
Action Item

1-5-A Page 126 Pre-Shipment Test Configuration-4. Jan 96 is the first HSI test. No breadboard is available on or before this date. Review HSI breadboard activity.

Response

The Payload/Spacecraft Simulator (PSS) scheduled for support of HSI I&T will be made available soon enough (mid June 95) to interface with the TRWLIS breadboard control electronics assembly.

This breadboard is planned to have the same design as the HSI control electronics assembly and will provide early verification of the interface with the PSS before HSI testing begins in July/August 95.

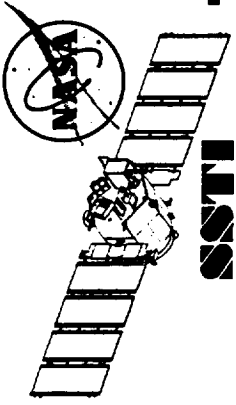


Integration and Test SSTI Test Bed



Integrate subsystem components before system level integration

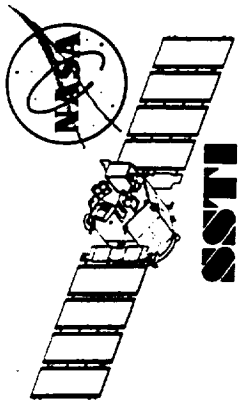
- Data Management Subsystem (DMS) and HSI are highest risk items
 - Spacecraft Computer (R3000)
 - Solid State Recorder (SSR)
 - Data Interface Unit (DIU)
 - 1553B Data Bus
 - Flight software
- Early checkout of test sets, test software and procedures
 - DMS Cmd and TLM (Data base verification)
 - ACS test set and test sequences (TOMS derivative)
 - Closed loop command and TLM tests



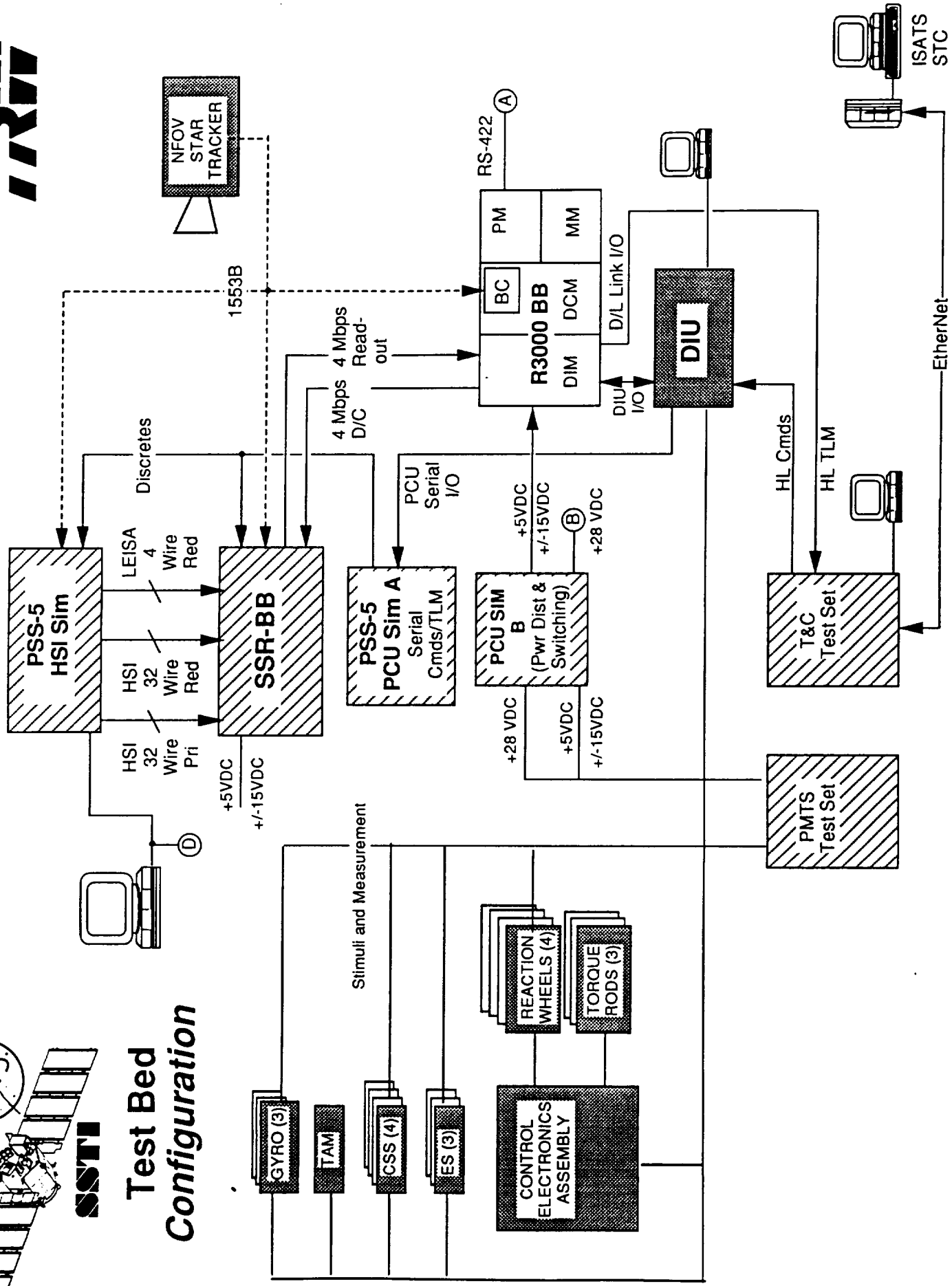
Integration and Test SSTI Test Bed

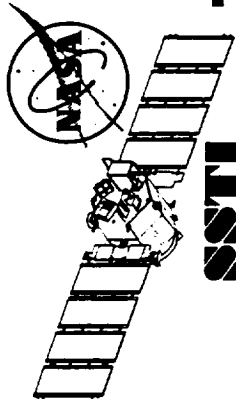


- Utilize the same test tools scheduled for system level integration and test
 - No dead end engineering tasks
 - No dead end test hardware or software developed
 - Supports both unit level test program and DMS and HSI integration at Space Park
 - * Payload and Spacecraft Simulators (SSTI unique)
 - * Telemetry Command Monitor
 - * System Test Controller (ISATS TOMS-EP derivative)
- Develop a test program which integrates the test tools early in the test program
 - R3000 breadboard and DIU simulator with:
 - * Payload and Spacecraft Simulator
 - * Telemetry and Command Test Set
 - * System Test Controller (ISATS)
 - * ACS flight instruments



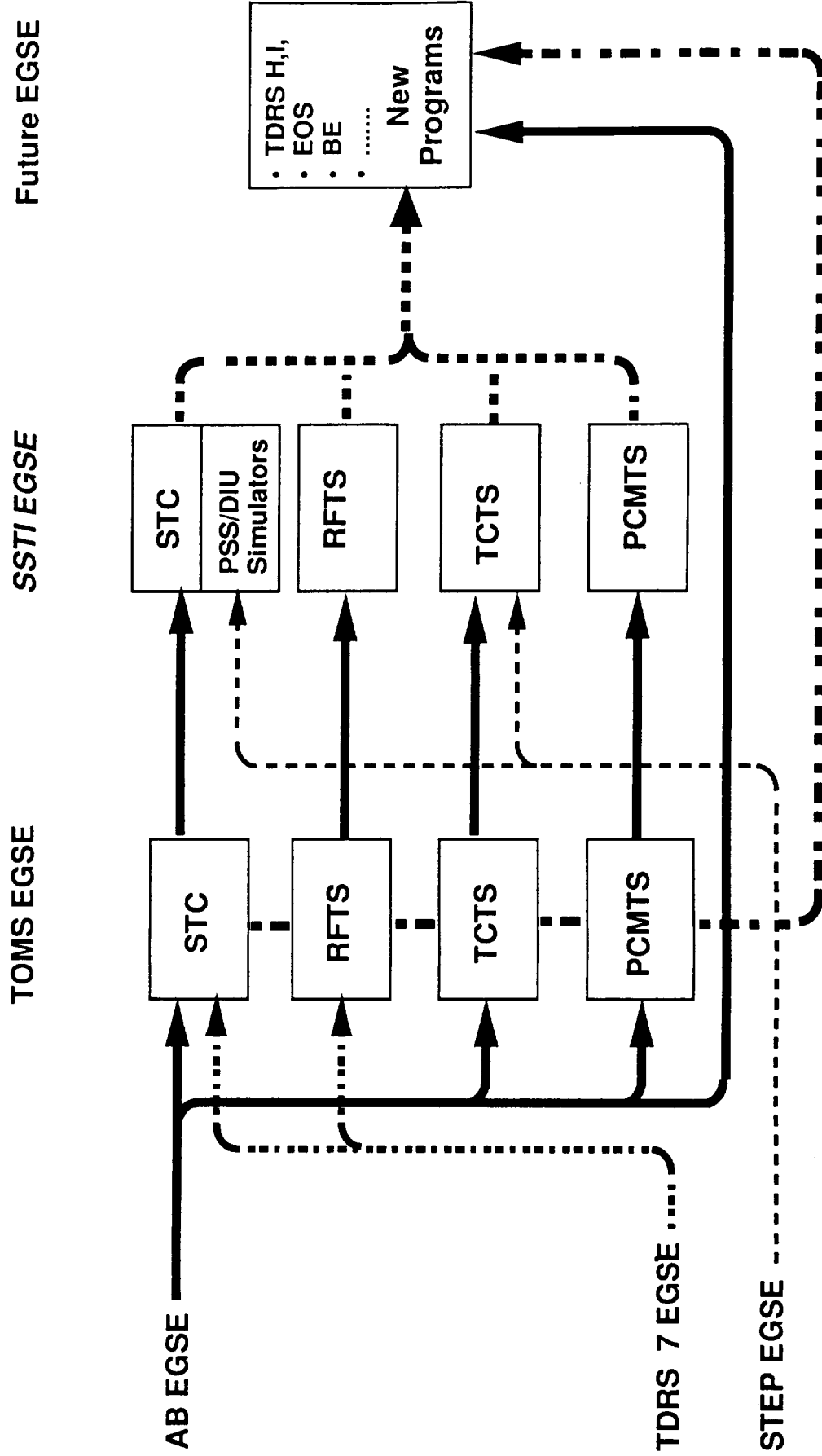
Test Bed Configuration

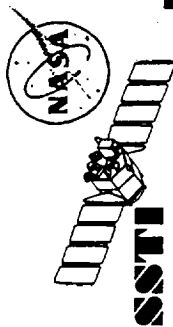




Integration and Test

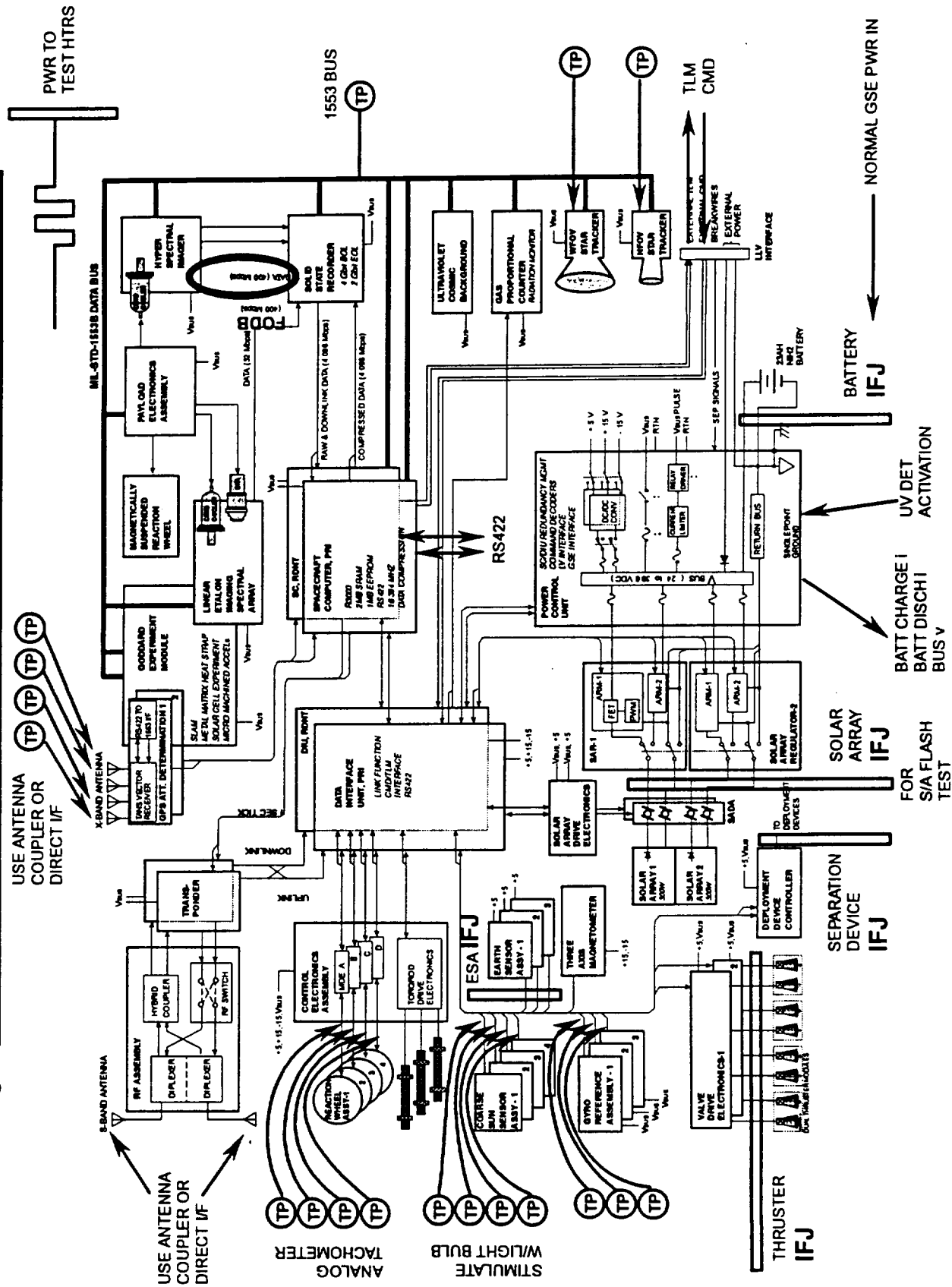
SSTI EGSE Heritage and Applications

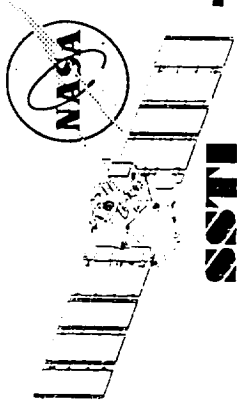




EGSE INTERFACE

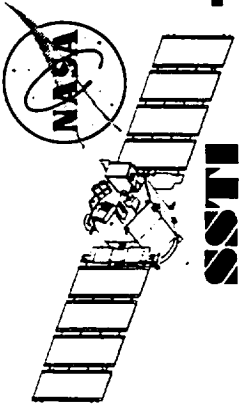
TRW





Small Satellite Technology Initiative Electrical Ground Support Equipment (SSTI EGSE)

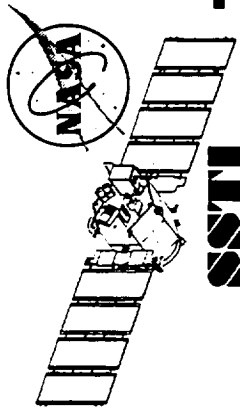
K. Cha
Jan, 95



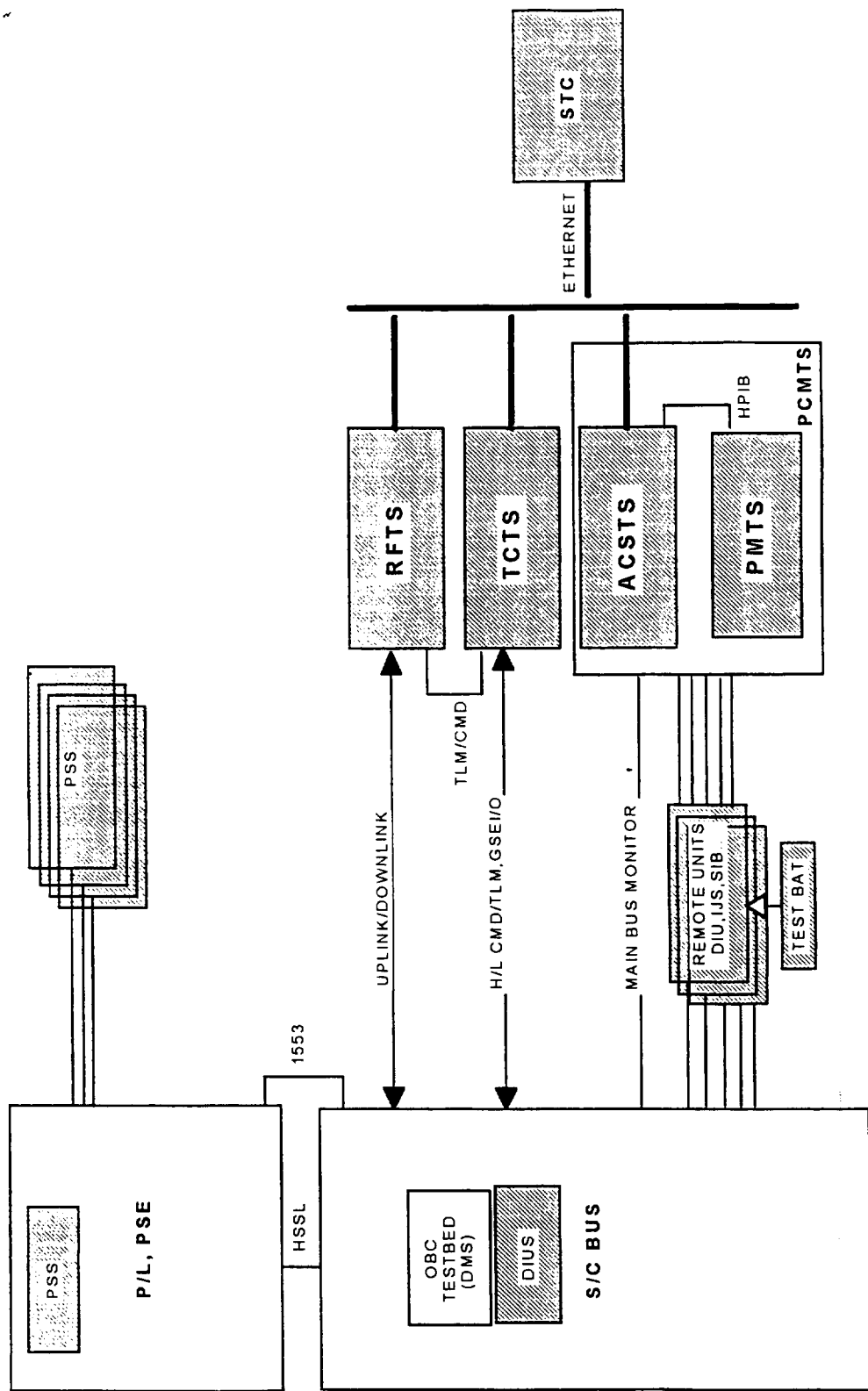
SSTI EGSE Overview

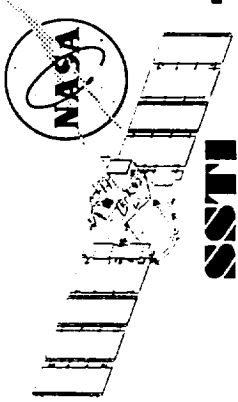


- The SSTI EGSE shall provide electrical interface and data processing support during integration, test and launch of the SSTI satellite. The supported electrical interfaces shall include power, deployment monitoring, attitude control and link services.
- In addition to supporting satellite integration & test (I/T), the SSTI EGSE shall also provide support to major subsystems I/T to allow their parallel development.
- SSTI EGSE Major Components
 - Telemetry and Command Test Set (TCTS)
 - RF Test Set (RFTS)
 - System Test Controller (STC) with ISATS (STC)
 - ACS Test Set (ACSTS)
 - Power and Monitor Test Set (PMTS)
 - Payload & Spacecraft Simulator (PSS)
 - Data Interface Unit Simulator (DIUS)



SSTI EGSE Top Level Block Diagram





SSTI EGSE Design Heritage and Concept

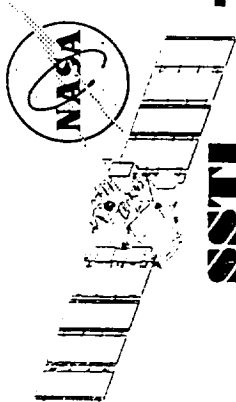


- The majority of the components are upgraded or exact design from previous and ongoing EGSE such as TOMS, BE/BP and DSP heritage.

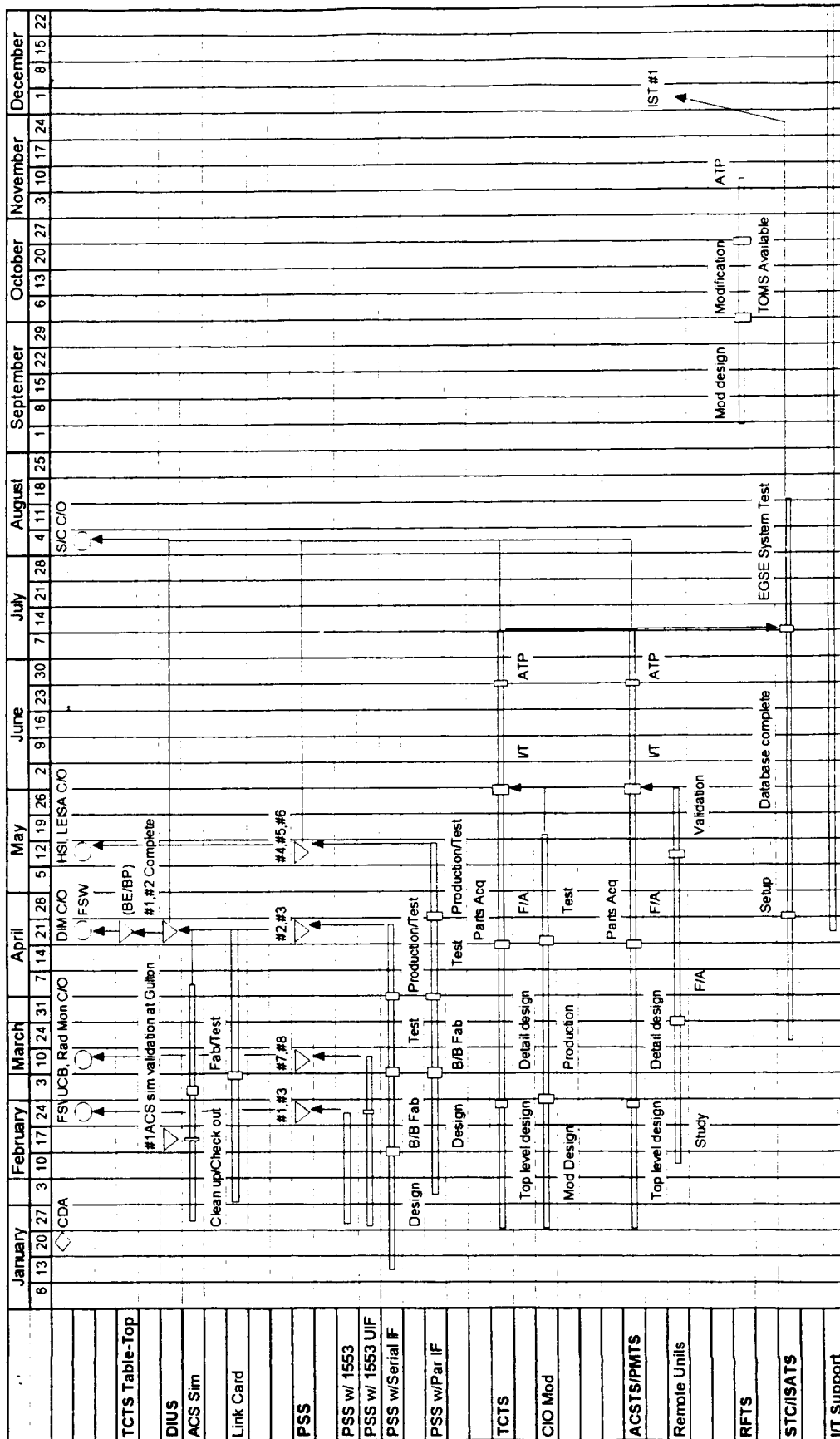
	Design baseline	Design Ratio	Comments
TCTS	DSP/BE/BP	Low	New TLM Format, CMD format unchanged from TOMS
RFTS	TOMS	Very Low	New data rate (2M and 8K)
STC	Generic	Low	New database
ACSTS	DSP/TOMS	Med to Low	Replace XTM with Labview/ New SADE I/F
PMTS	DSP/TOMS	Low	Minor adjustment for delta requirements
PSS	New	100 %	Simulate P/L and S/C subsystems
DIUS	SSTI IRAD	Med	Link function need to be completed

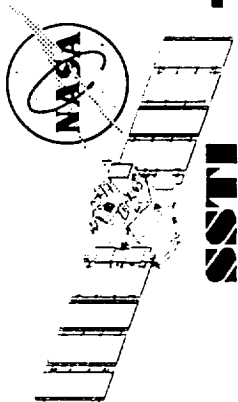
Design Ratio = New Design or Modification/Total design

- **Design Concept**
 - Generic modular Design with COTS preferred (Spare on-hand)
 - Flexible configuration in user friendly manner (Graphical interface preferred)
 - Minimize new design wherever possible
 - Maximize self test capability (provide major signals loop back capability)



SSTI EGSE Top Level Schedule



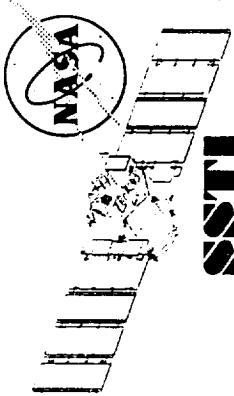


SSTI EGSE Description (STC w/ ISATS)



- Central data processing subsystem which performs Automated Procedures (Aps) in integral system environment with spacecraft by initiating commands and post-processing SOH telemetry. STC provides archive, limit check, and data trend analysis capabilities with overall control of both EGSE and the spacecraft.
- SSTI ISATS will be hosted by VAX 4000-505 system under VMS operating system connected to all other test sets over ethernet (DecNet).
- Major Components

Major Item	Buy	Make-New	Use	Comments
STC	X			
Jupiter	X			
Printers..	X			
ISATS			X	EDI generated database to be transferred

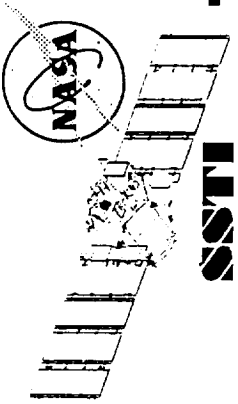


SSTI EGSE Description (TCTS)



- The TCTS provides digital link data interface and front end data processing for command and telemetry between STC and spacecraft (via RFTS for Up/Downlink) with following major functions:
 1. Provide Remote command and Telemetry interface to STC
 2. Local command generation and echo verification
 3. Simulated Telemetry generation, Telemetry decoding and frame sync
 4. H/L CMD/TLM interface to S/C and baseband signal handling for RFTS
- TCTS is equipped with Sun workstation host under Unix and core functional equipment packaged in VME chassis with real-time target processor under VxWork.

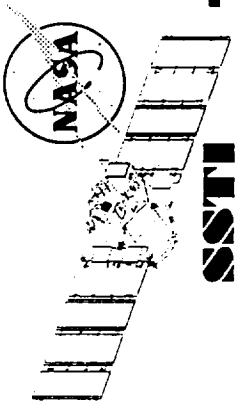
Major Item	Buy	Make-New	Make-Mod	Comments
TCP	X			
TLM Simulator	X			
TLM Decom	X			
Bit Sync	X			
Viterbi Enc/Dec	X			
PSK Modem	X			
CMD I/O			X	Need to enhance Serial Command function
Switch Card	X			
TCTS S/W			X	Basically adoption from DSP



SSTI EGSE Description (RFTS)



- The RFTS performs Uplink modulation and Downlink demodulation for SSTI with baseband signals from/to TCTS, as well as providing link performance measurement capability. The RF signal characteristics are as follow:
 1. Launch / Early Orbit secondary mode RF Telemetry (8 kbps NRZ-M Convolution Encoded Rate 1/2 BPSK onto 1.024 MHz then PM 1 rad onto 2287 MHz)
 2. On-Orbit Primary mode RF Telemetry (2.048 Mbps NRZ-M Convolution Encoded Rate 1/2 BPSK onto 2287 MHz)
 3. STDN RF Commanding (2 kbps NRZ-S BPSK onto 16 kHz then PM 1 rad onto 2106 MHz)
- No components list is shown since TOMS RFTS will be used as is with very minor modification.



SSTI EGSE Description (ACSTS)



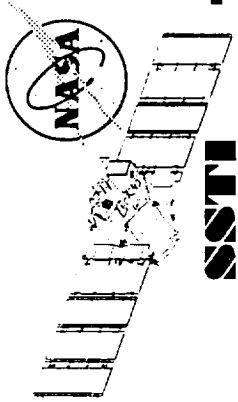
- The ACSTS provides instruments and equipment required to perform GN&C subsystem test of the SSTI during fixed based and system level for following SSTI components:

4 Reaction Wheels.
3 Earth Sensors.
3 gyros.
3 Torque-Rods.
2 GPS receivers.

4 Course Sun Sensors.
3 TAM sensor channels.
2 Solar Array Drive Assemblies (SADA).
2 Valve Drive Electronics (VDE's).

- The ACSTS is equipped with Labview hosted by Sun workstation which drives VXI chassis cards. The ACSTS also provides control and status of the PMTS.

Major Item	Buy	Make-New	Use-Mod	Comments
ACP	X			
Analog I/O	X			In: 39V, 8A, 3H-E Out: 23V, 11A
Counter I/O	X			In: 12 CK, 5Ga, 9Dir O 12CK, 19 Ga, 7 Dir
Serial I/O	X			2 Channels
1553 RT	X			Primary & Redundant
Mux/Switch	X			
ACS S/W			X	Procedure modification
Remote Units	X		X	VDE Load SIM, GPS, Hall Effects, ...

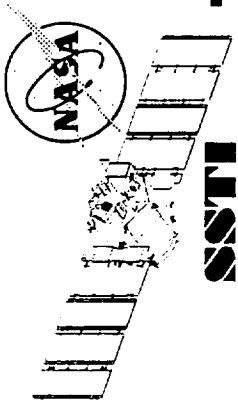


SSTI EGSE Description (PMTS)



- The PMTS provides and monitors DC power to the SSTI spacecraft main bus through the inputs of the Solar Array Regulators (SAR's), through the Launch Vehicle Interface (LVIF) or through the battery power bus. The battery power bus source shall be either a power supply, the test battery or the flight battery.
- In addition, the PMTS shall simulate and monitor the main bus load, monitor a battery discharge load and continuously monitor and measure all deployment device channels through simulated loads.
- Other than power supplies and load simulators, the PMTS components will be packaged into a VXI chassis. All PMTS units provide remote control and status capability to ACSTS via HPIB interface.

Major Item	Buy	Make-New	Use-Mod	Comments
SAS	X			HP6684
Battery SIM	X			HP6032
SAR Load	X			HP6050
Battery Charge	X			HP6038
Battery Discharge	X			HP6051
Remote Units			X	Diode Iso Unit, IFJ Sim, S/C IF Buf,

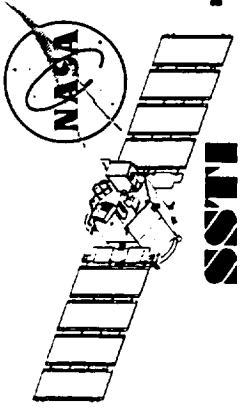


SSTI EGSE Description (DIUS)



- The DIUS simulates the DIU interface to OBC-DIM to allow parallel development of various subsystem including flight S/W. Static response unit for I/O cards were developed and demonstrated as a part of SSTI IRAD.
- Major Functions
 - Simulate DIU backplane bus (Similar to 80C86 bus)
 - Receive and handle Command data interface for OBC-DIM
 - Dynamic Response (TBD)
- The DIUS is a stand-alone PC (486) with two custom cards which runs under 16-bit ISA in DOS environment.

Major Item	Buy	Make-New	Use-Mod	Comments
PC-486	X			
ACS Sim			X	Need to clean-up (Need to be validated at Gulton)
CMD Decoder		X		Need to complete test
S/W			X	TBD for dynamic response, otherwise use as is



SSSI EGSE Description (PSS)

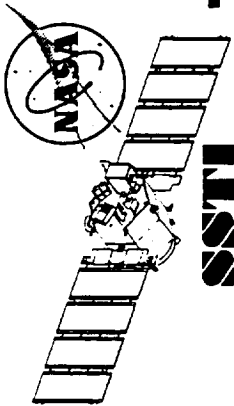


- The PSS simulates the interfaces and required test functions of the major units within SSSI, such as SSR (PSE & P/L), OBC (S/C) and so forth.
- The interfaces simulated by the PSS are
 - Parallel interfaces (HSI-SSR, LEISA-SSR)
 - Serial interfaces (SSR-OBC)
 - 1553 interfaces (overall)
 - Discrete interfaces (overall)

Major Components

Major Item	Buy	Make-New	Use-Mod	Comments
PC-486	X			
Parallel IF card		X		
Serial IF card		X		
Discrete IO card	X			
1553 BC	X			
1553 RT/BM	X			
SW		X		

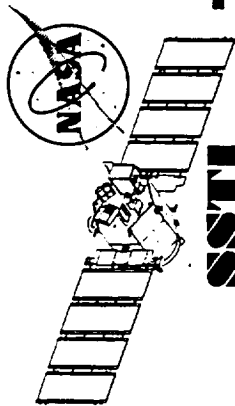
- Detailed design description attached as appendix A.



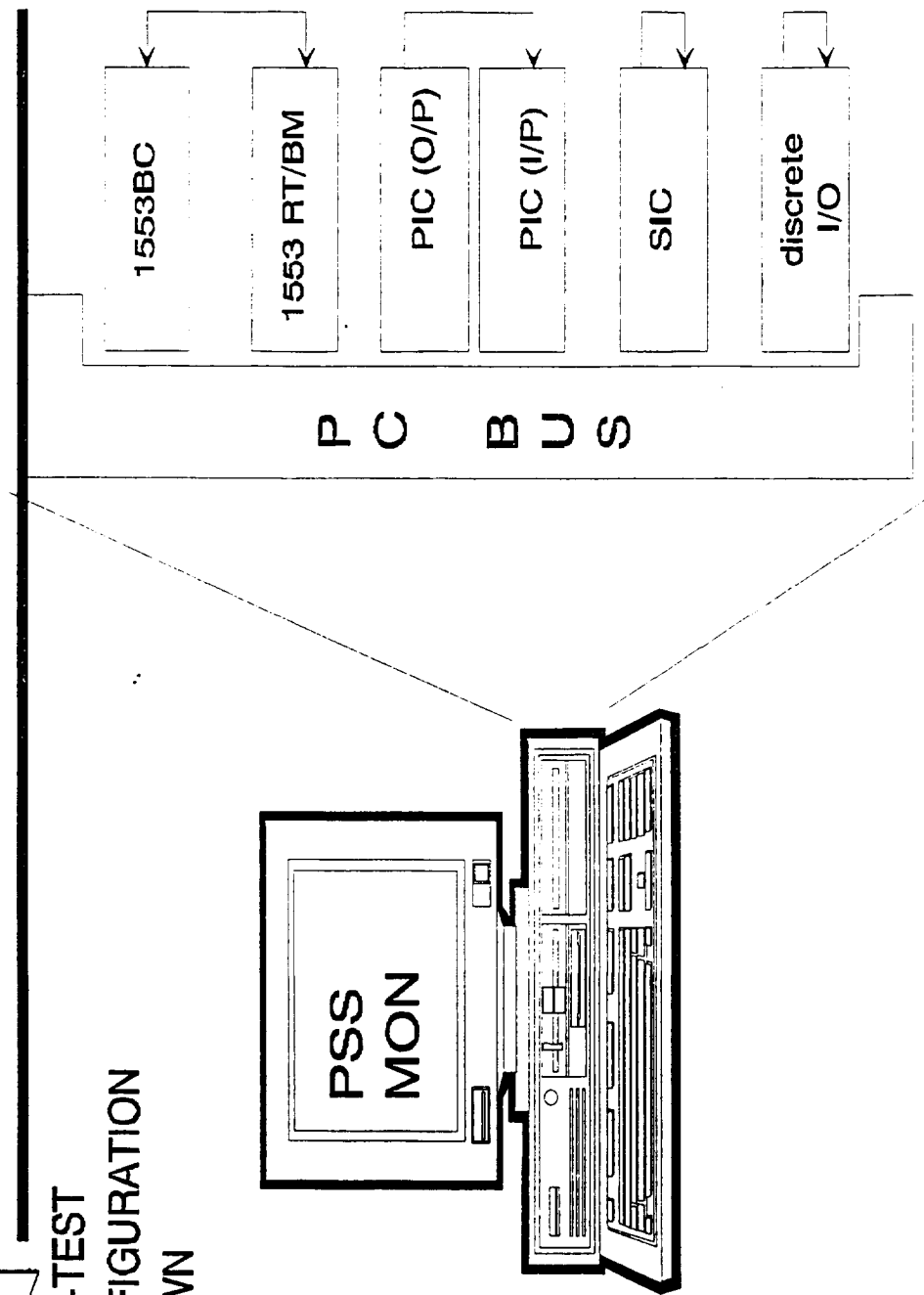
APPENDIX A

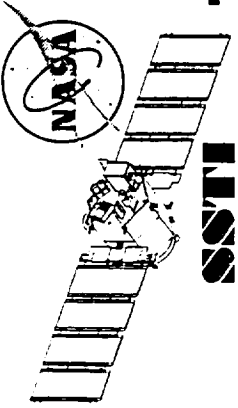


PSS DESIGN DESCRIPTION DATA PACKAGE



PSS Block Diagram





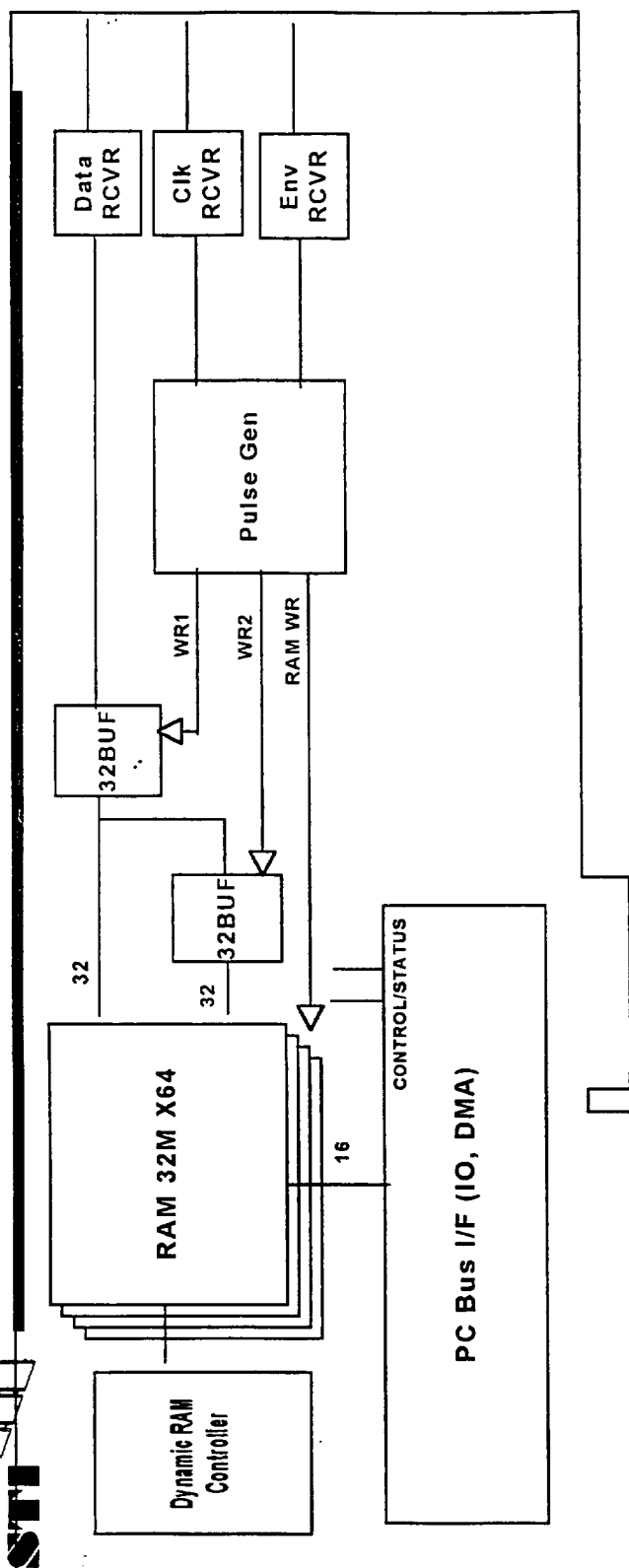
Parallel Input Card (PIC) Description

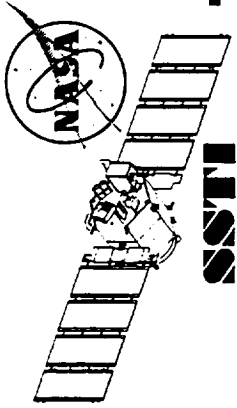


- The PIC simulates SSR interface for the HSI and the LEISA by providing memory buffer for display and data pathway to HSI or LEISA workstation.
- The PIC provides 2 Giga-Bits of memory space by double depth and width of 16M X 32 DRAM (SIM package) to form 32M X 64
 - External interface is still performed in 32 bits wide format, where internal backplane interface is 16 bits wide.
 - Double buffer latching scheme as done for SSR performed internally to establish effective rate operable to dynamic RAM speed
- Parallel Output card (Test-Aid) will be designed for PIC validation. POC emulates HSI or LEISA by transmitting pre-loaded data in repeating fashion.



Parallel Input Card (PIC) Block Diagram

[illegible]



Parallel Input Card (PIC) Interfaces

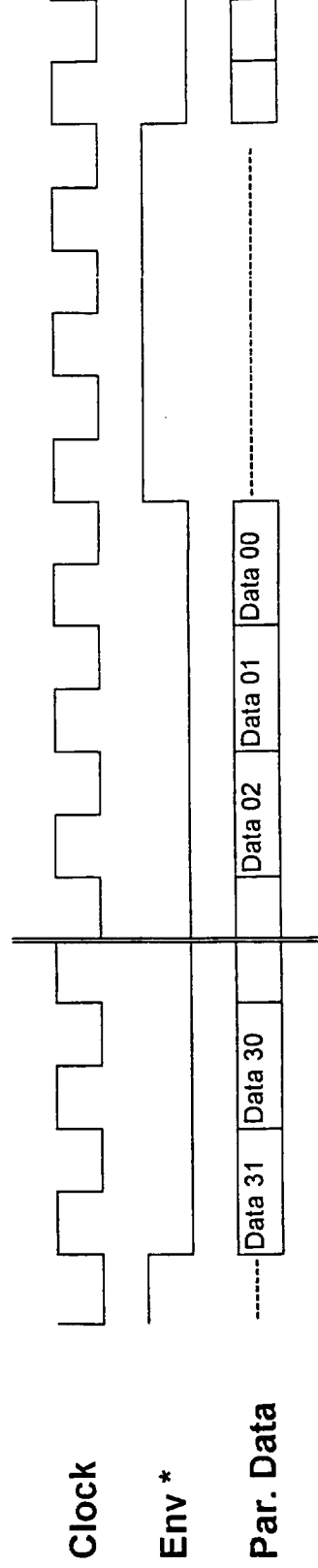


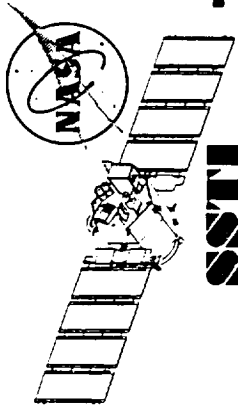
PIC provides following input interfaces:

- 1) 32-bits parallel bus data
- 2) Free running clock at max 13.75 Mhz
- 3) Data Envelope

All signals are RS-422 level with 26LS31/32 devices. 120 Ohm line to line termination will be made on board for inputs. Incoming shields will be terminated to signal ground at the connector

Interface Timing Diagram





Parallel Input Card (PIC) Design



- The PIC will be an I/O mapped memory card

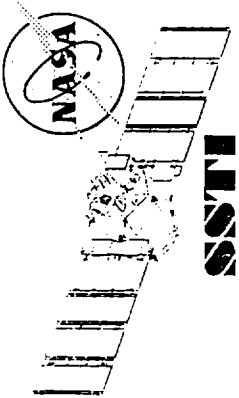
Address Map for PIC

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Function
CARD ADDRESS					x	x	x	x	x	x	x	Card Address
					x	x	x	x	x	x	1	High Byte
04XXh RESERVED					x	x	x	x	x	1	x	High word
BY ISA SPEC					x	x	0	0	1	1/0	1/0	Data field contains RAM address
					0	0	0	1/0	1	x	x	Data Acq. Start/Finish address*
					0	0	1	0	0	x	x	Data Read from RAM
					0	1	0	0	0	x	x	Card Control
					1	0	0	0	0	x	x	Card Status

Example

0 0 0 0 1 0 x Requesting lower 16bits of RAM finished address
 0 0 1 0 0 0 x Data read of selected RAM location

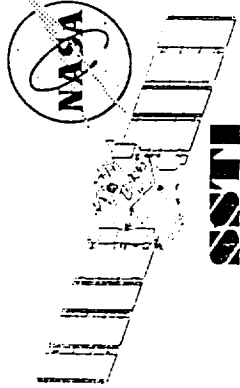
* Card will automatically increment address during continuous read



Parallel Output Card (POC) Description



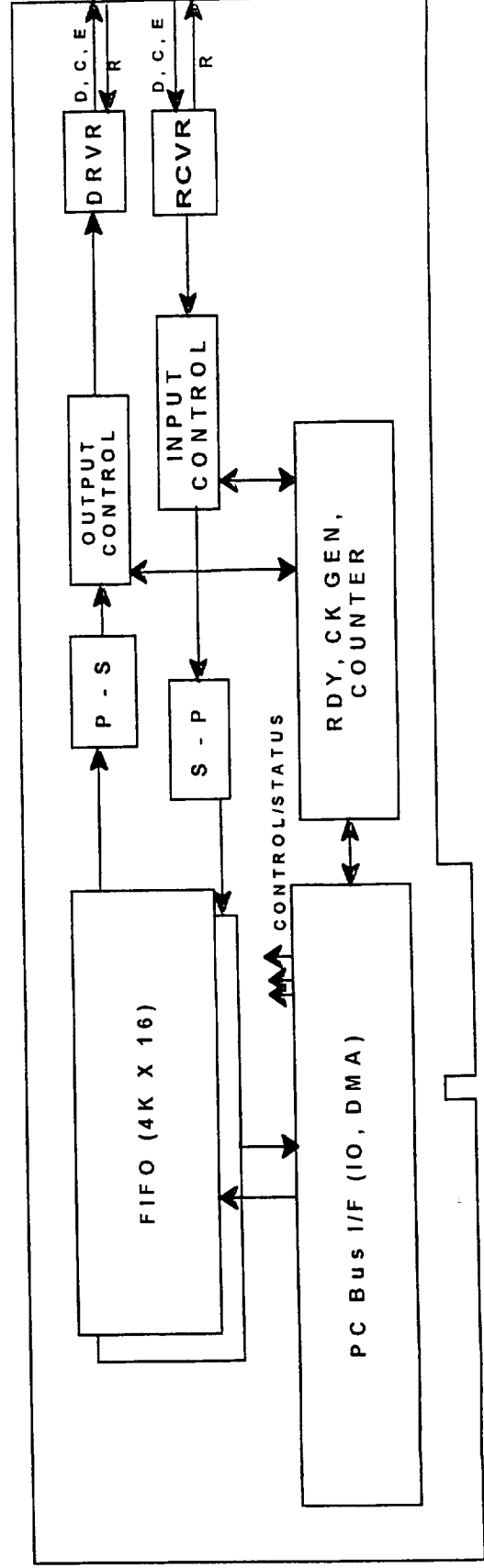
- One wire-wrapped card will be generated for PIC validation as a test-aid. Other PSS components provide self test (validation) capability.
- POC transmits data in HSI or LEISA mode (32 bits or 4 bits).
- The board will be loaded with Dual port RAM (8 Mbyte minimum) in which data will be repeated in continuous mode. In burst mode data will be transmitted in multiple of SSR package size (1920 bits)

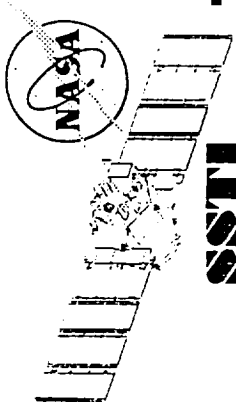


Serial Interface Card (SIC) Description



- The SIC simulates the High Speed Serial interface between the OBC and the SSR. The card can be configured as OBC or SSR as required.
- The SIC provides self test capability by on- or off- board loop back.
- The SIC provides 4K X 16 FIFO on board which can generate continuous serial stream when needed. (Effective required bus transfer rate of 256K) Otherwise, S/W initiates burst transmission of S/W controlled block size of SSR package.

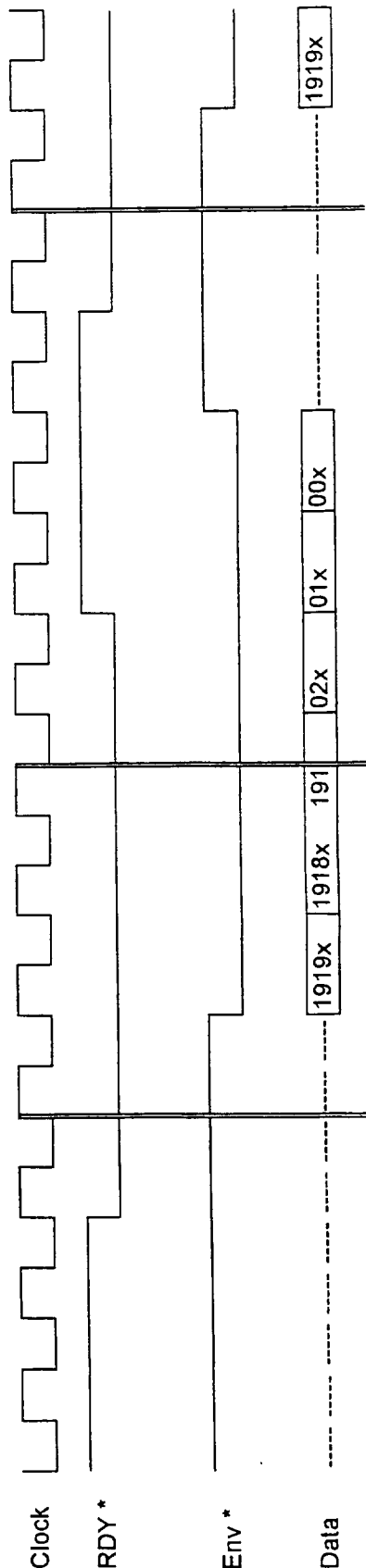




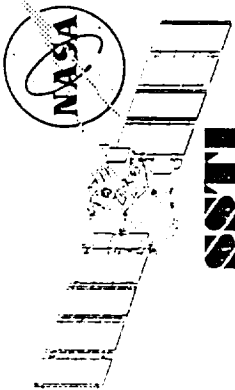
Serial I/F Card (SIC) Interfaces



- Input ...
 - 1) Serial Data
 - 2) Free running clock at 4.096 MHz
 - 3) Data Envelope
 - 4) Device RDY (When SSR is simulated, otherwise always RDY)
- Output
 - 1) Serial Data (1920 bits per SSR package/The count managed by S/W)
 - 2) Free running clock at 4.096 Mhz (Int/Ext, Ext=derived from input clock)
 - 3) Data Envelope
 - 4) Device RDY (When interfacing with SSR, set it always RDY)



RDY to ENV 1 uSec minimum, RDY before ENV 1uSec minimum
 Sixty 32 bit words per SSR package = 1920 bits



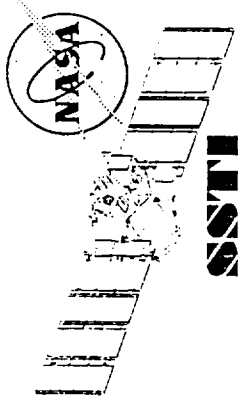
Serial I/F Card (SIC) Design



A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Function	...
CARD ADDRESS												Card Address	
					x	x	x	x	x	x	1	High Byte	
04XX RESERVED												High word	
BY ISA SPEC												Address Output FIFO	
					x	0	0	1	0	x	x	Address Input FIFO	
					x	0	1	0	0	x	x	Card Control	
					x	1	0	0	0	x	x	Card Status	

Data Bit																R/W	Function
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Card Mode (1=CPC, 0=SIC)
															x	R/W	Reset Card
																W	Clock Sel (1=Int 0= Ext)
																R/W	Clock Rate
																R/W	RDY Output Enable/Dis
																R/W	RDY Input Enable/Dis
																R/W	Local Loop back En/Dis
																R	FIFO Status (EF,HF,FF)
																W	Start Transmission
																W	Stop Transmission
																W	Interrupt Reg Clear
																R	Command Reg/SIC busy
																W	Command/SIC Int Mask
																	Spare
																	Spare

SIC Interrupts at receipt of 1920 bits, CPC interrupts at receipt of valid command

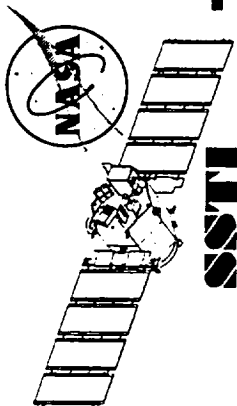


PSS Applications

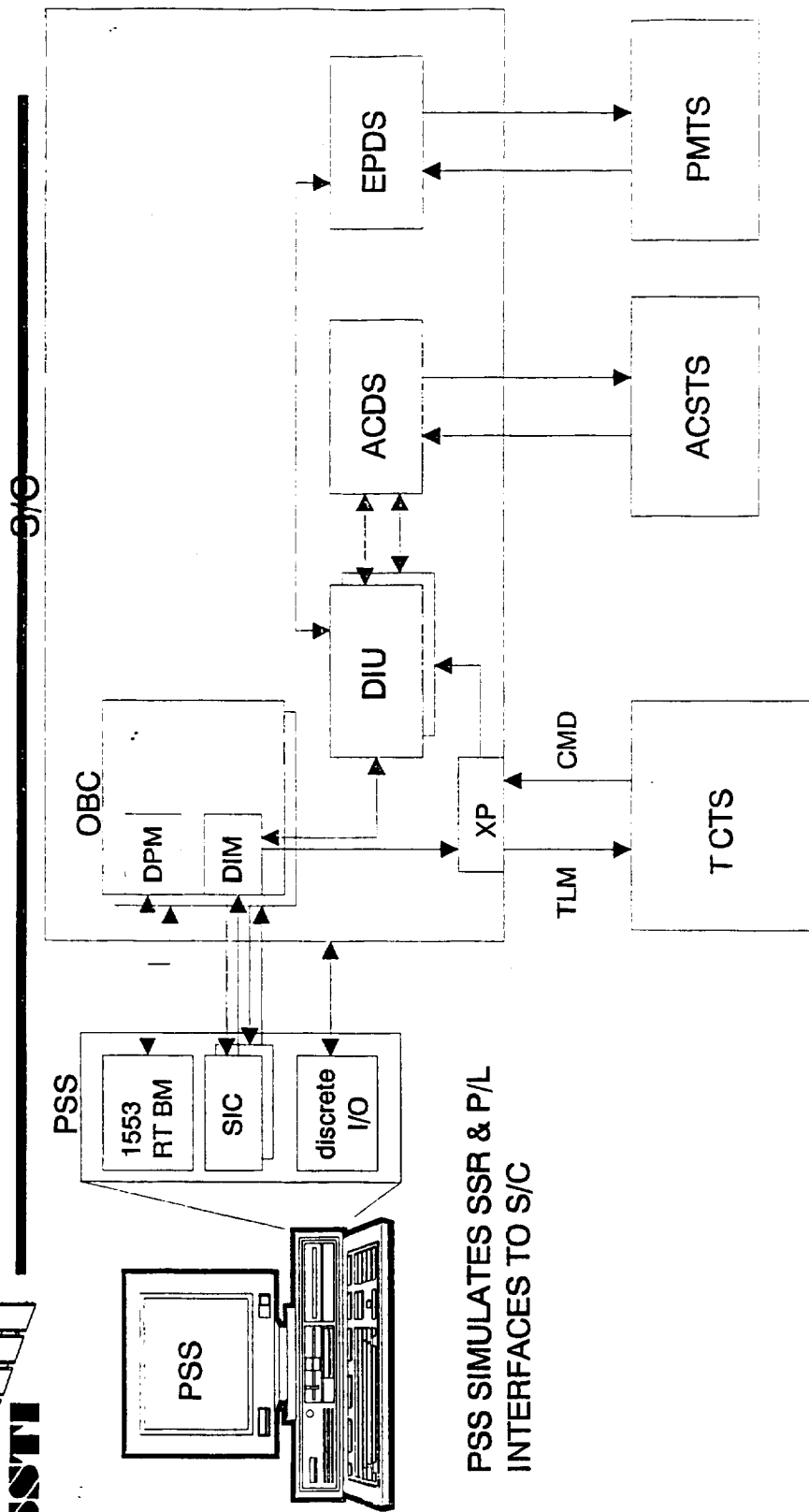


- The PSS shall be configured as needed for each application with common hardware and software.
- During initialization the PSS software shall prompt the user to configure the test environment.

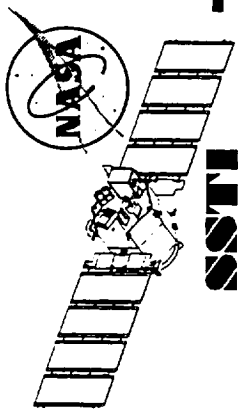
	USAGE	SIMULATING	INTERFACES
UNIT 1	S/W DEVELOPMENT	SSR, MISC	ALL (XFER TO MAIN SYSTEM I/T)
UNIT 2	S/W DEVELOPMENT	SSR, MISC	SERIAL, 1553RT/BM, DISCRETE
UNIT 3	OBC & DMS I/T	SSR	2xSERIAL, 1553RT/BM, DISCRETE
UNIT 4	Spare Unit	All	4xPARALLEL, 2xSERIAL, 1553BC, 1553RT/BM, DISCRETE
UNIT 5	HSI I/T	SSR	2xPARALLEL, 1553BC, 1553RT/BM, DISCRETE
UNIT 6	LEISA I/T	SSR	2xPARALLEL, 1553BC, 1553RT/BM, DISCRETE
UNIT 7	UCB I/T	OBC	1553BC, 1553RT/BM
UNIT 8	RAD MON	OBC	1553BC, 1553RT/BM



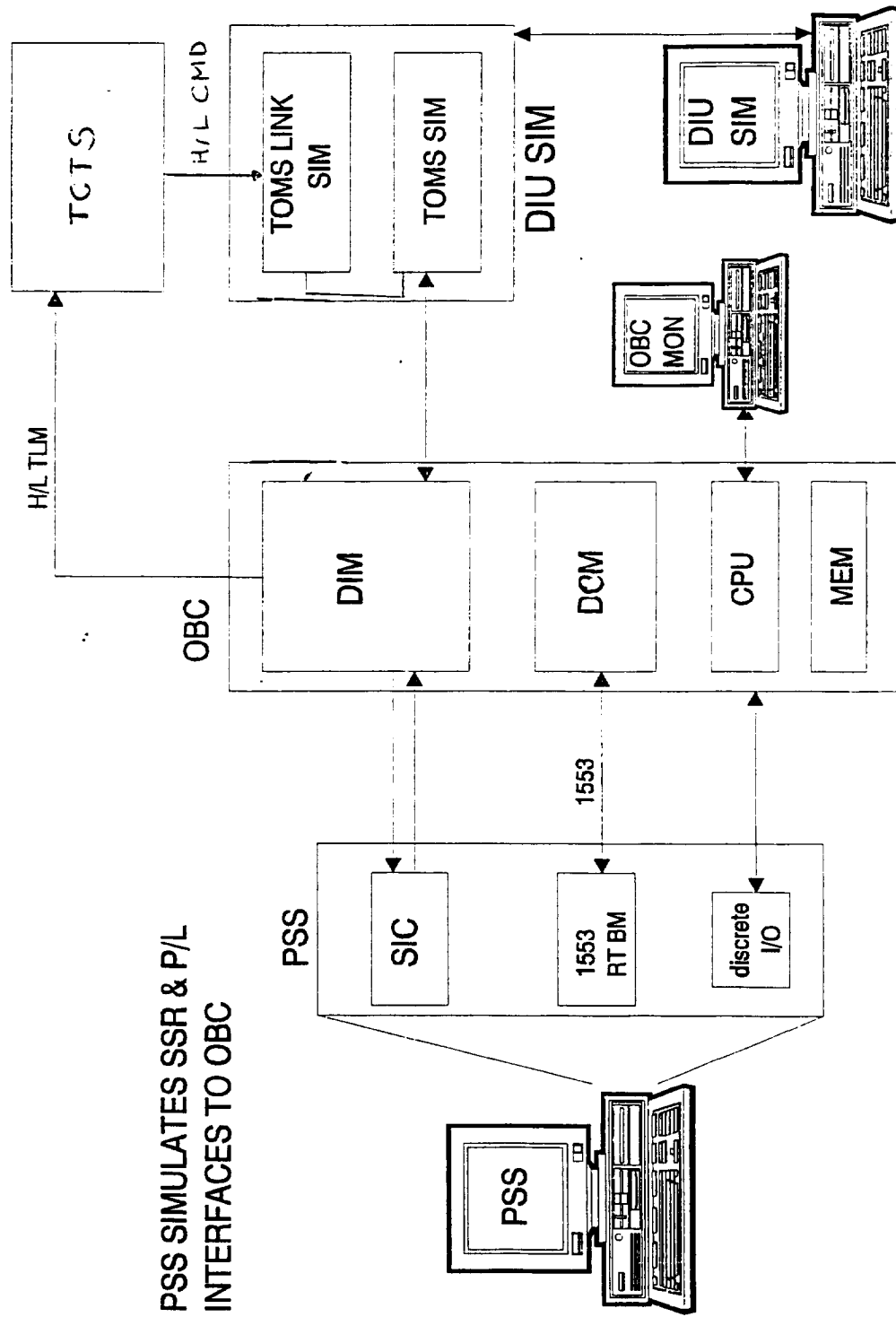
PSS Applications- Main System I/T

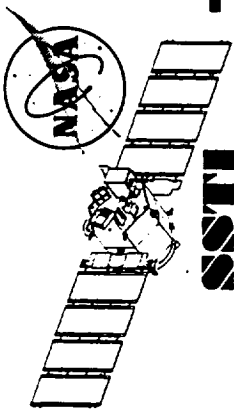


PSS SIMULATES SSR & P/L
INTERFACES TO S/C



PSS Applications- S/w Development & OBC I/T

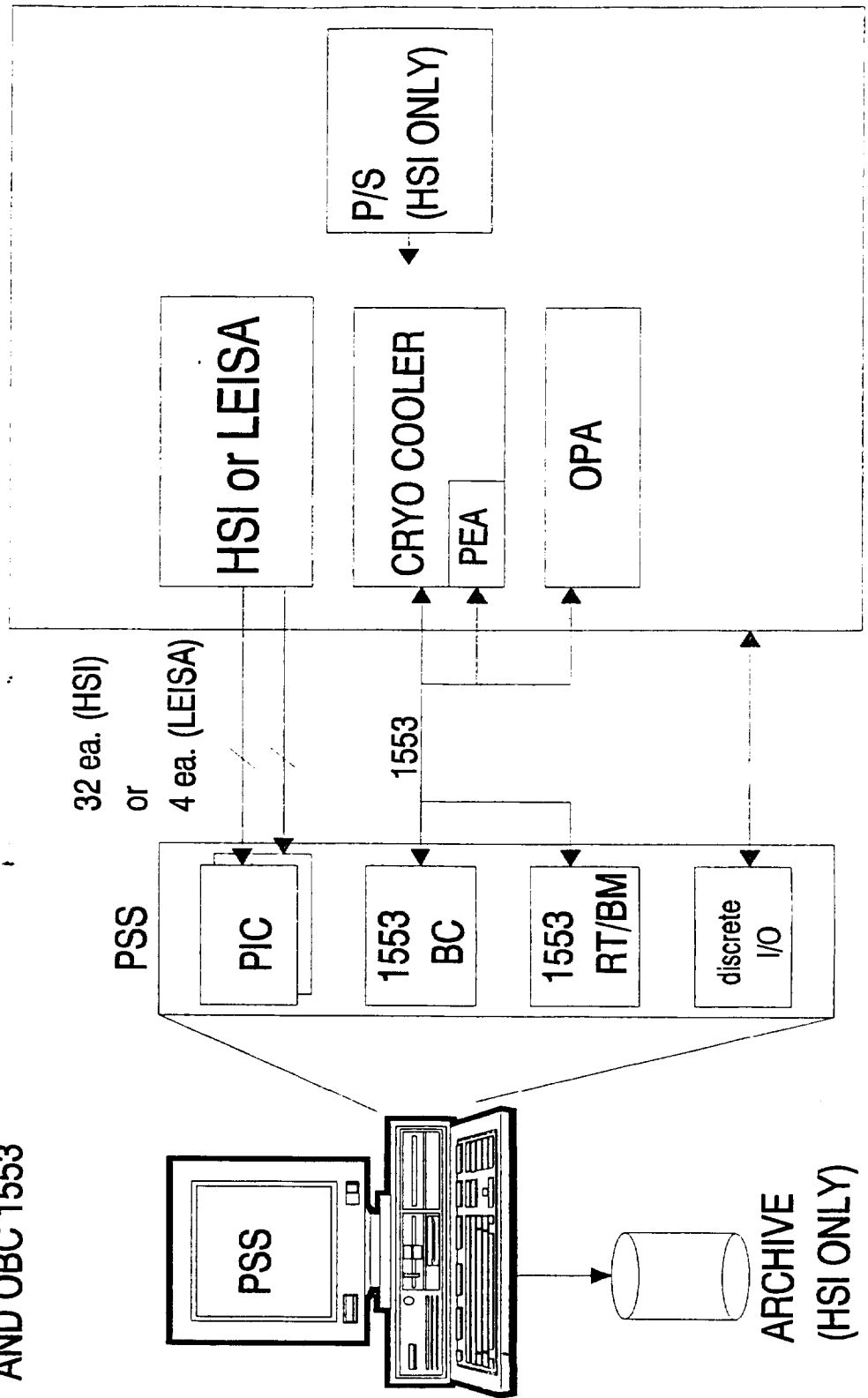




PSS Applications- HSI & LEISA I/T



PSS SIMULATES SSR I/F TO UUT
AND OBC 1553



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13. ABSTRACT (Maximum 200 words)
The Critical Design Audit package is the final detailed design package which provides a comprehensive description of the SSTI mission. This package includes the program overview, the system requirements, the science and applications activities, the ground segment development, the assembly, integration and test description, the payload and technology demonstrations, and the spacecraft bus subsystems. Publication and presentation of this document marks the final requirements and design freeze for SSTI.

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